



Ampere® Altra® 64-Bit Multi-Core Processor Platform Hardware Design Specification

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Contents

1.	Altra Overview	8
1.1	Processor Subsystem.....	8
1.2	Performance and Power	8
1.3	Memory.....	8
1.4	Connectivity.....	9
1.5	System Resources.....	9
1.6	Technology and Functionality	9
1.7	Process Technology	9
1.8	Internal Blocks	10
1.9	Package Overview	10
2.	Altra Platform Building Blocks	12
2.1	Dual-Socket Systems	12
2.2	Memory Subsystem.....	13
2.2.1	Linear Topology	13
2.2.2	Signal Connectivity	14
2.2.3	DIMM Connectors	16
2.3	PCIe/CCIX Subsystem	16
2.3.1	PCIe/CCIX Ports and Lane Configurations.....	16
2.3.2	Reference Clock Scheme.....	17
2.3.3	PCIe Reset Scheme.....	18
2.3.4	PCIe Card Presence Detection	18
2.3.5	PCIe Hot-Plug Support.....	19
2.3.6	Schematic Design Guide.....	20
2.3.7	Signal Groups.....	23
2.4	Networking.....	24
2.5	Storage	25
2.6	CCIX Acceleration	25
3.	Management Subsystem.....	26
3.1	Baseboard Management Controller (BMC)	27
3.1.1	Overview of AST2500	27
3.1.2	BMC Features on Altra	28
3.2	I/O Interfaces Between Two Sockets and BMC	39
3.3	BMC on Dual-Socket (2P) Systems	42
3.4	BMC on Single-Socket (1P) Systems.....	42
4.	Power Supply Design Guidelines	43



Contents (continued)

4.1	Power Supply Design Requirements	43
4.1.1	Physical Design	43
4.1.2	Decoupling Requirements to Achieve Target Impedance	45
4.1.3	Voltage Regulator Power Efficiency	47
4.1.4	Min/Max Voltages for I/O Power Rails	47
4.1.5	I/O Voltage Filter Requirements	47
4.1.6	Power Supply Management	47
4.1.7	Power Sequencing	49
4.1.8	Dynamic Voltage and Frequency Scaling (DVFS)	51
4.2	VRD Implementation using Texas Instruments Devices	52
4.2.1	Overview of TI Voltage Regulators	52
4.2.2	Reference Layout	53
4.3	VRD Implementation using Infineon Devices	54
4.3.1	Overview of IR Voltage Regulators	54
4.3.2	Reference Layout	55
4.4	Power Integrity Simulations	55
4.4.1	Simulation Results	56
5.	Clock Distribution	63
5.1	System Clock Design Guidelines	63
5.1.1	Connectivity	63
5.1.2	CPU System Clock Requirements	63
5.1.3	Schematic Guides	64
5.2	Miscellaneous Clock Design Guidelines	64
5.2.1	TMR Clock	64
5.2.2	UART Clock	64
5.2.3	Termination if Unused	64
6.	Reset Distribution	65
6.1	Altra PERST Encode Table	65
6.2	Design Guidelines	70
6.2.1	Connectivity	70
6.2.2	Altra System Reset Requirements	70
7.	Miscellaneous I/O Interfaces	71
7.1	I2C/SMBus Usage	71
7.1.1	Design Guidelines	71
7.1.2	Termination if Unused	74



Contents (continued)

7.1.3	Recommended Device	74
7.1.4	Layout Guidelines	74
7.2	UART	75
7.2.1	Design Guidelines	75
7.3	QSPI	77
7.3.1	Design Guidelines	77
7.3.2	Termination if Unused	78
7.3.3	Recommended Devices	78
7.4	GPIOs and GPIs	79
7.5	JTAG (Daisy Chain for 2P Systems)	84
7.5.1	Design Guidelines	84
8.	System Boot	86
8.1	EEPROM Programming and SMpro Boot-up	86
8.1.1	EEPROM Programming Sequence	86
8.1.2	SMpro Boot-up Sequence	87
8.2	UEFI Programming and Boot-up	89
8.2.1	UEFI Programming Sequence	89
8.2.2	UEFI Boot-up Sequence	89
9.	Hardware Bring-up Guide	90
9.1	Component Inspection Checks	90
9.2	Power Supply and GND Short Checks	90
9.3	Power Rails Checks	91
9.4	Power Sequence Measurement	92
9.5	Clock Signals Checks	92
10.	Bibliography	94
11.	Document Revision History	95



Figures

Figure 1: Altra Block Diagram	8
Figure 2: Altra Internal Blocks	10
Figure 3: Altra Package Size and Pad Array	11
Figure 4: Altra Package Partition (Preliminary)	11
Figure 5: Dual-Socket Interconnection via CCIX	12
Figure 6: System Memory Topology with One DIMM per Channel	13
Figure 7: System Memory Topology with Two DIMMs per Channel	13
Figure 8: DDR4 Signal Connectivity for One DIMM per Channel	14
Figure 9: DDR4 Signal Connectivity for Two DIMMs per Channel	15
Figure 10: Type A Root Complex's x16 SerDes Configuration	16
Figure 11: PCIe Card Presence Detection	18
Figure 12: PCIe Card Hot-Plug Connection Diagram	19
Figure 13: PCIe NVMe SSD Hot-Plug Connection Diagram	19
Figure 14: Ferrite Beads and Decoupling Capacitor for Analog Power Pins	21
Figure 15: PCIe I2C Connections	22
Figure 16: PCIe 4.0 Root Complex Connectivity Diagram	22
Figure 17: CCIX Connection Between Two Sockets	23
Figure 18: OCP NIC 3.0 Reference Diagram	24
Figure 19: Onboard M.2 NVMe and Backplane U.2 NVMe	25
Figure 20: HBA Card Connectivity with Backplane for SAS/SATA Devices	25
Figure 21: CCIX Implementation using PCIe x16 Ports	25
Figure 22: BMC Functional Diagram	27
Figure 23: BMC DDR4 SDRAM Block Diagram	28
Figure 24: BMC SPI Diagram	28
Figure 25: BMC I2C Network	29
Figure 26: UART Connection Diagram	30
Figure 27: BMC Fan Control and Monitor	31
Figure 28: BMC Power Rails Monitor	32
Figure 29: BMC VGA Display Port	33
Figure 30: BMC Network Interfaces	33
Figure 31: BMC USB Interfaces	34
Figure 32: BMC JTAG Master Programming Diagram	35
Figure 33: User Indicator LEDs	38
Figure 34: I/O Interfaces Between Two Sockets and BMC	41
Figure 35: AST2500 BMC Block Diagram for Single-socket Platforms	42



Figures (continued)

Figure 36: Altra Power Supply Diagram	43
Figure 37: Altra Power Supply Sequencing	49
Figure 38: CPLD Controlled Power Up Sequence	50
Figure 39: System Configuration using Two Voltage Regulators	51
Figure 40: VRD Power Diagram for Dual-Socket Platform using TI Devices	52
Figure 41: VRD Power Diagram for Dual-Socket Platforms using Infineon Devices	54
Figure 42: Voltage Drop Example (Idealized, Not to Scale)	56
Figure 43: Voltage Drop Example (Idealized, Not to Scale)	57
Figure 44: VDDC_PCP PCB-Only Frequency Domain Impedance Plot	57
Figure 45: VDDC_SOC Max Current Ramp Rate and Current Step	58
Figure 46: VDDC_SOC PCB-Only Frequency Domain Impedance Plot	59
Figure 47: VDD_RCA PCB-Only Frequency Domain Impedance Plot – with 10 mΩ Ferrite Bead	61
Figure 48: VDDQ_0123/VDDQ_4567 Max Current Ramp Rate and Current Step	61
Figure 49: VDDQ_0123 PCB-Only Frequency Domain Impedance Plot	62
Figure 50: Differential Reference Clock Block Diagram	63
Figure 51: Altra REFCLK Termination	63
Figure 52: System Reset Diagram	70
Figure 53: I2C Block Diagram for Dual-Socket Platforms	71
Figure 54: UART Block Diagram for Dual-Socket Platforms	75
Figure 55: CPU's 2-Wire UART Connection to Header	76
Figure 56: SPI-NOR and TPM Connection Diagram	77
Figure 57: JTAG Daisy Chain Within Altra	84
Figure 58: JTAG Daisy-Chain Connection in 2P Systems	85
Figure 59: System Boot for Dual-Socket Platforms	88



Tables

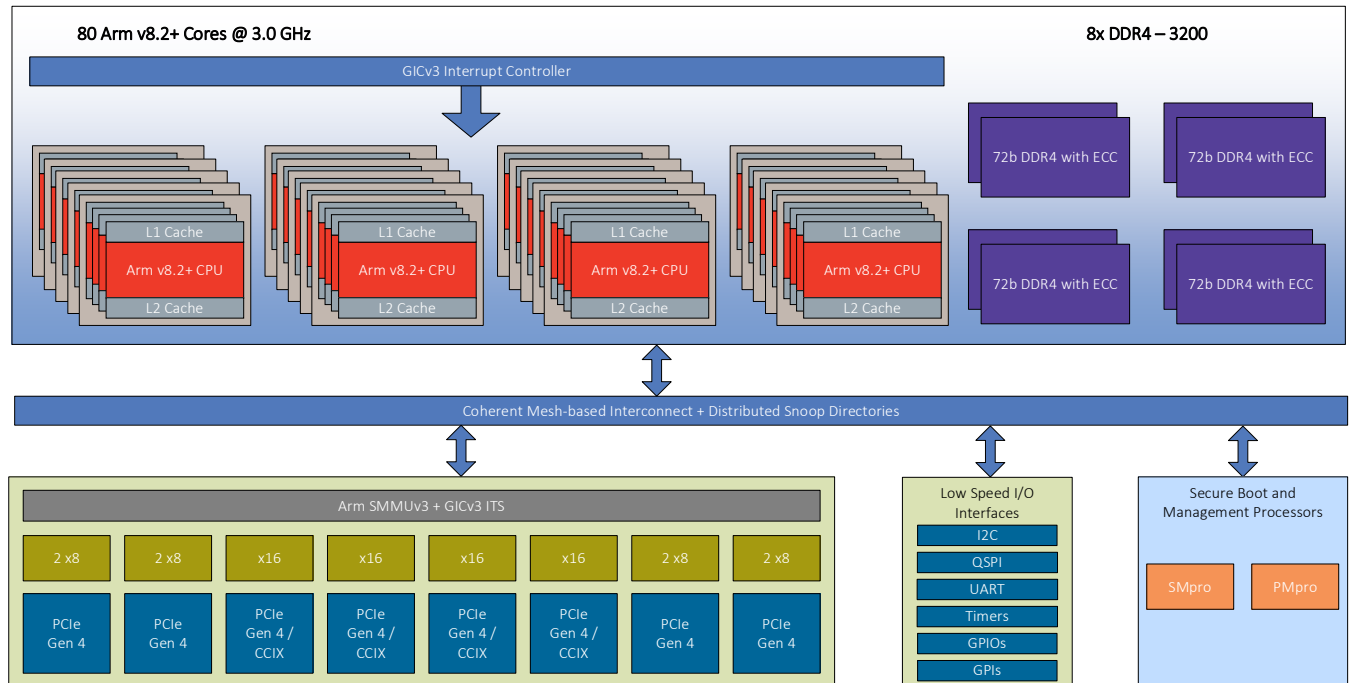
Table 1: Example of Supply Bypass Capacitors	20
Table 2: PCIe Signals	23
Table 3: BMC Functions	26
Table 4: JTAG Signal Description	35
Table 5: JTAG Mode Selection	36
Table 6: GPIO Interfaces Between Two Sockets and BMC.....	39
Table 7: Power Rails Design.....	43
Table 8: +0V75_PCP_S0 Decoupling Capacitors	45
Table 9: +0V75_VDDC_SOC_S0 Decoupling Capacitors.....	46
Table 10: +0V85_RCA_S0 Decoupling Capacitors	46
Table 11: +1V2_DDQ0123_S0 Decoupling Capacitor	47
Table 12: PCP Power Ramp Steps.....	56
Table 13: VDDC_SOC Max Current Ramp Rate and Current Step	58
Table 14: VDDC_RCA Mission-mode Steady-state Current Calculation Based on PHY Data Book Specifications	60
Table 15: VDDQ_0123/4567 Max Current Ramp Rate and Current Step.....	61
Table 16: Altra PERST Encode.....	65
Table 17: I2C Signals	72
Table 18: Altra I2C Interfaces	72
Table 19: Altra UART Allocation	76
Table 20: Altra GPIOs Assignment.....	79
Table 21: VCC and GND Short Checks (Unit: Ω)	90
Table 22: Mainboard Power Rails' Voltage Measurement	91
Table 23: Mainboard Clock Frequency Measurement.....	92



1. Altra Overview

Figure 1 shows the Altra block diagram.

Figure 1: Altra Block Diagram



1.1 Processor Subsystem

- 80 Arm® v8.2+ 64-bit CPU cores at up to 3.30 GHz maximum
- 64 KB L1 I-cache, 64 KB L1 D-cache per core
- 1 MB L2 cache per core
- 32 MB System Level Cache (SLC)
- 2x full-width (128b) SIMD
- Coherent mesh-based interconnect
 - Distributed snoop filtering

1.2 Performance and Power

- SPECrate® 2017_int_base: 290
- TDP: 45 W to 250 W

1.3 Memory

- 8x 72-bit DDR4-3200 channels
- SECDED ECC, Symbol-based ECC, and DDR4 RAS features
- Up to 16 DIMMs and 4 TB/socket



1.4 Connectivity

- 128 lanes of PCIe Gen4
 - 8 x8 PCIe + 4 x16 PCIe/CCIX with Extended Speed Mode (ESM) support for data transfers at 20/25 GT/s
 - 48 controllers to support up to 32 x2 links
- 192 lanes in 2P configuration
- Coherent multi-socket support
- 4 CCIX links

1.5 System Resources

- Full interrupt virtualization (GICv3)
- Full I/O virtualization (SMMUv3)
- Enterprise server-class RAS

1.6 Technology and Functionality

- Armv8.2+, SBSA Level 4
- Advanced Power Management
 - Dynamic estimation, Turbo Gen2, Voltage droop mitigation

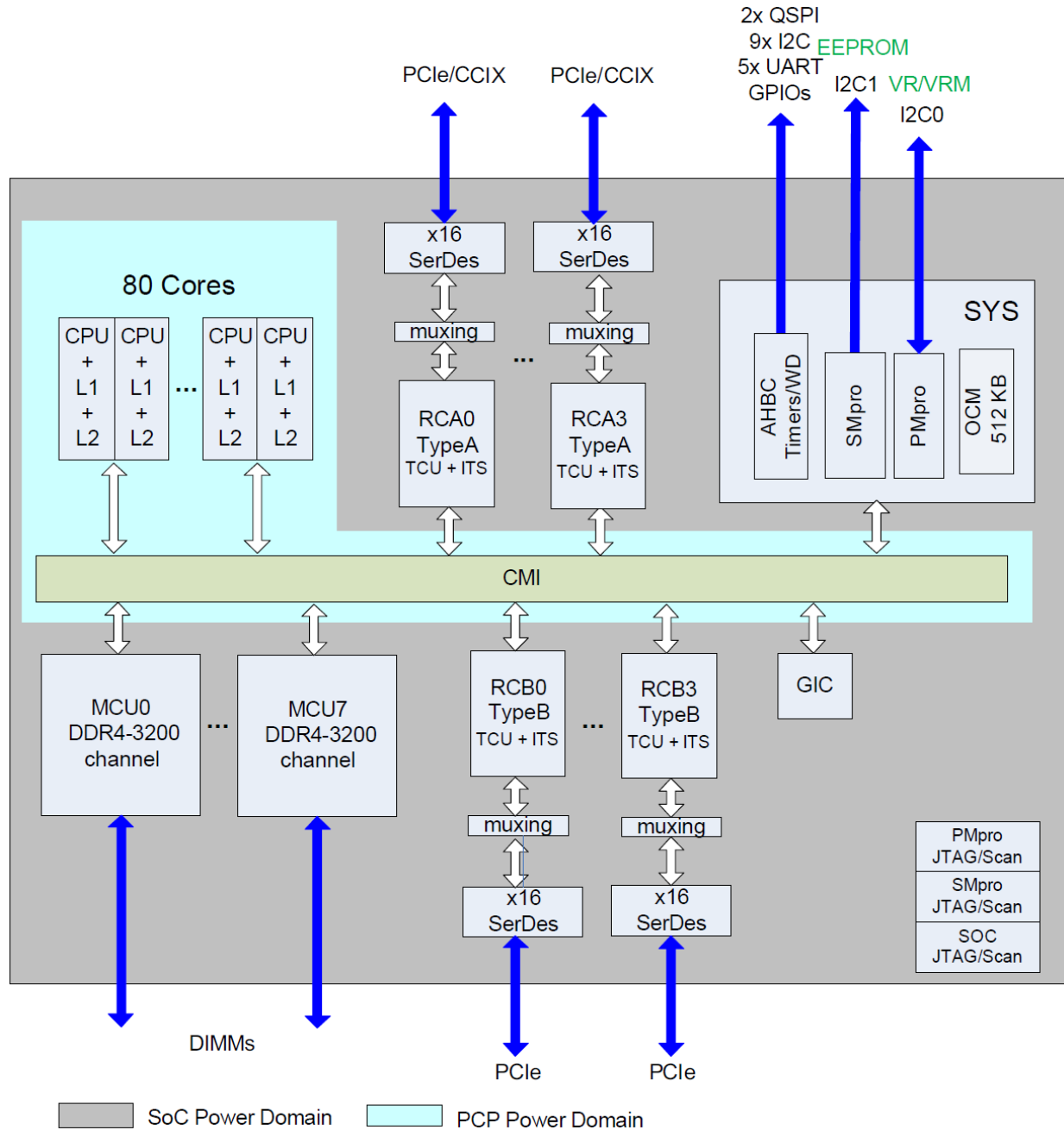
1.7 Process Technology

- TSMC 7 nm FinFET



1.8 Internal Blocks

Figure 2: Altra Internal Blocks



1.9 Package Overview

- Dimensions: 77.08 mm x 67.00 mm
- Pitch between pads: Hexagon Dx = 0.87 mm; Dy = 0.5 mm
- Total number of pads = 4926
- Number of columns Nx = 84; Number of rows Ny = 126
- PCB installation: Using socket
- POD and socket drawing: Refer to [Figure 3](#)



Figure 3: Altra Package Size and Pad Array

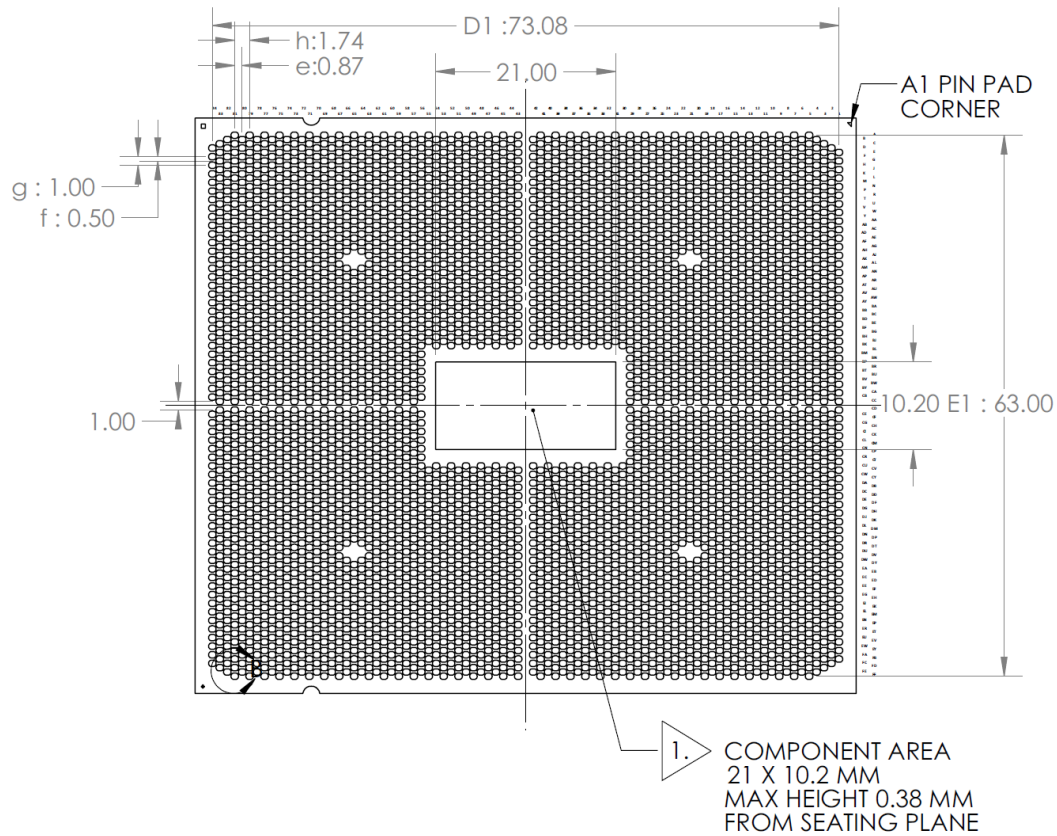
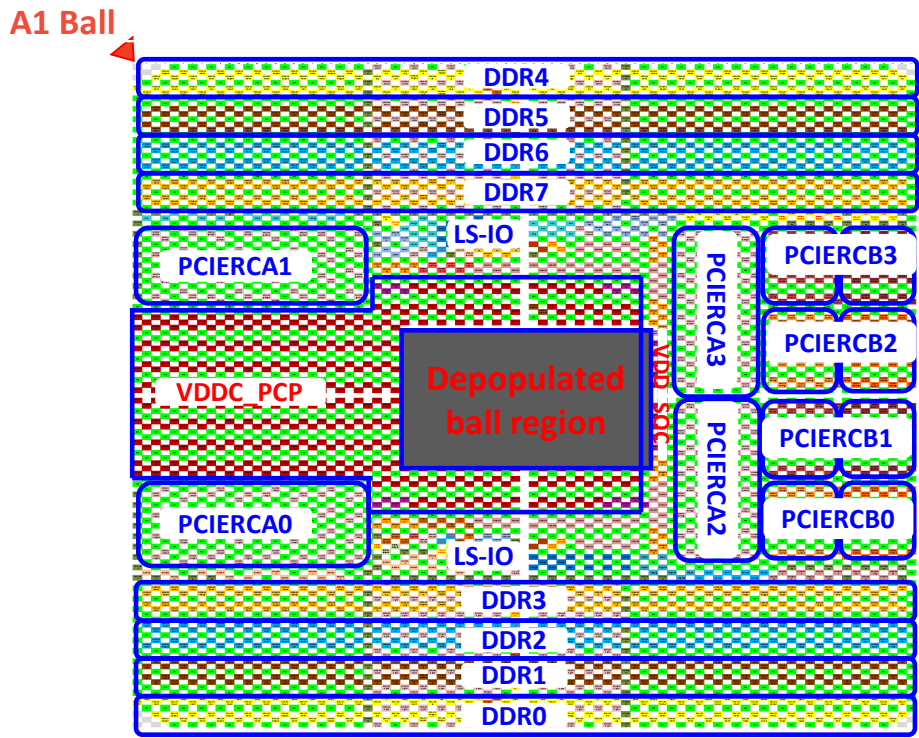


Figure 4: Altra Package Partition (Preliminary)





2.2 Memory Subsystem

2.2.1 Linear Topology

Figure 6 and Figure 7 illustrate the system memory topologies with 1DPC and 2DPC, respectively.

Figure 6: System Memory Topology with One DIMM per Channel

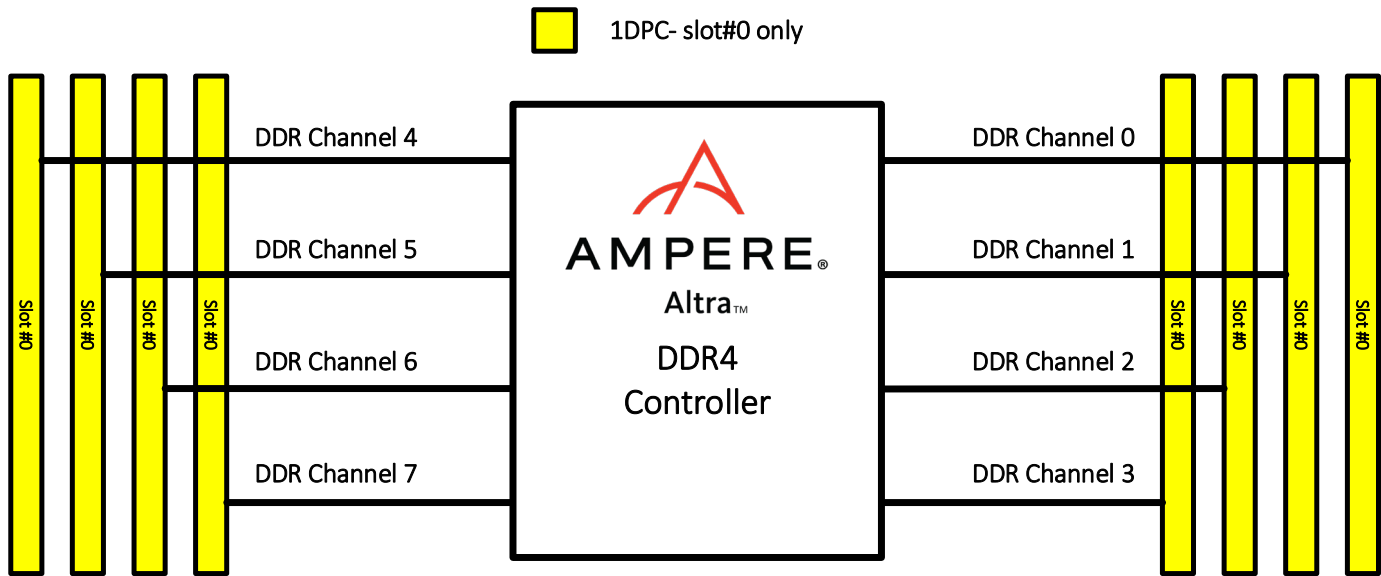
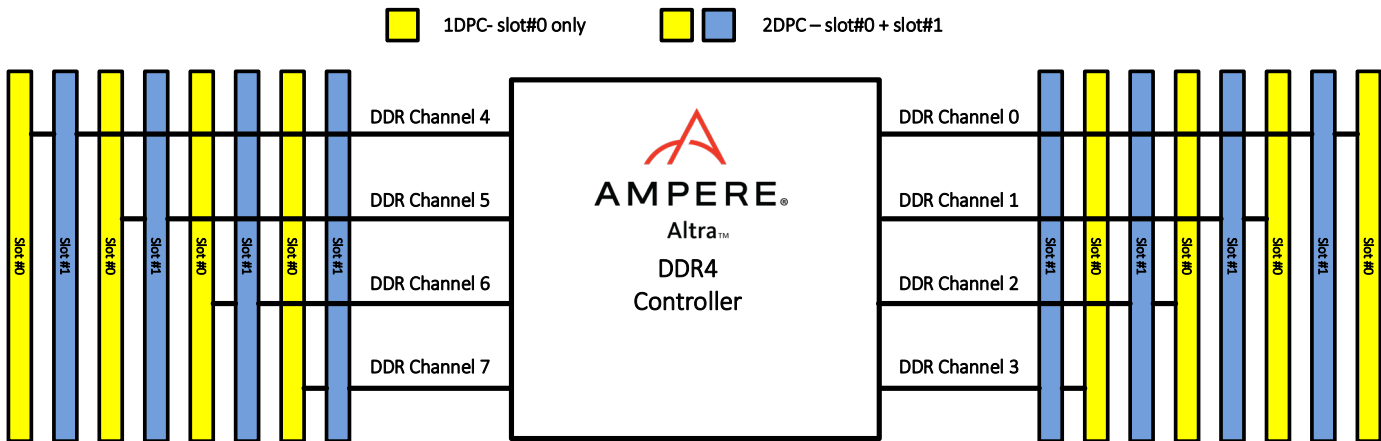


Figure 7: System Memory Topology with Two DIMMs per Channel





2.2.2 Signal Connectivity

Figure 8 and Figure 9 illustrate signal connectivity for 1DPC and 2DPC, respectively.

Figure 8: DDR4 Signal Connectivity for One DIMM per Channel

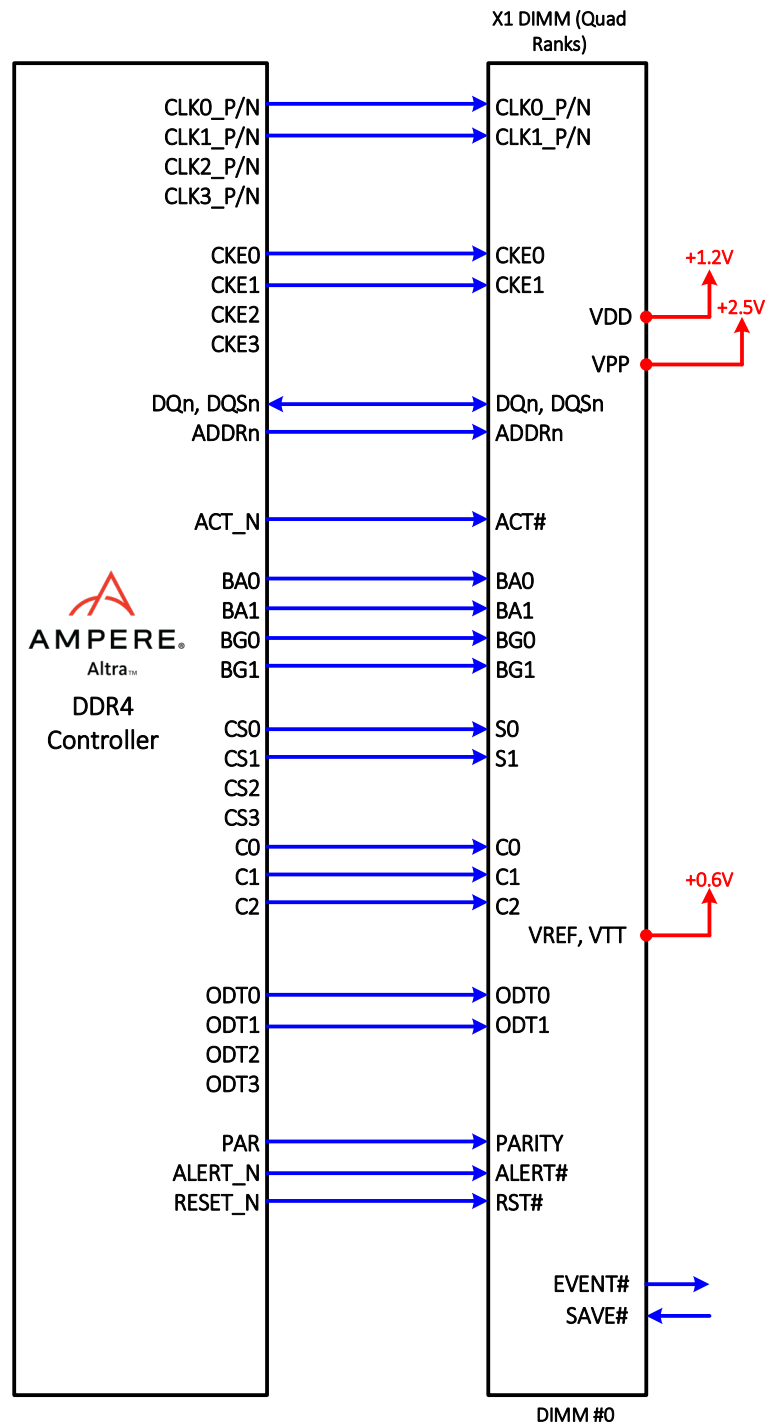
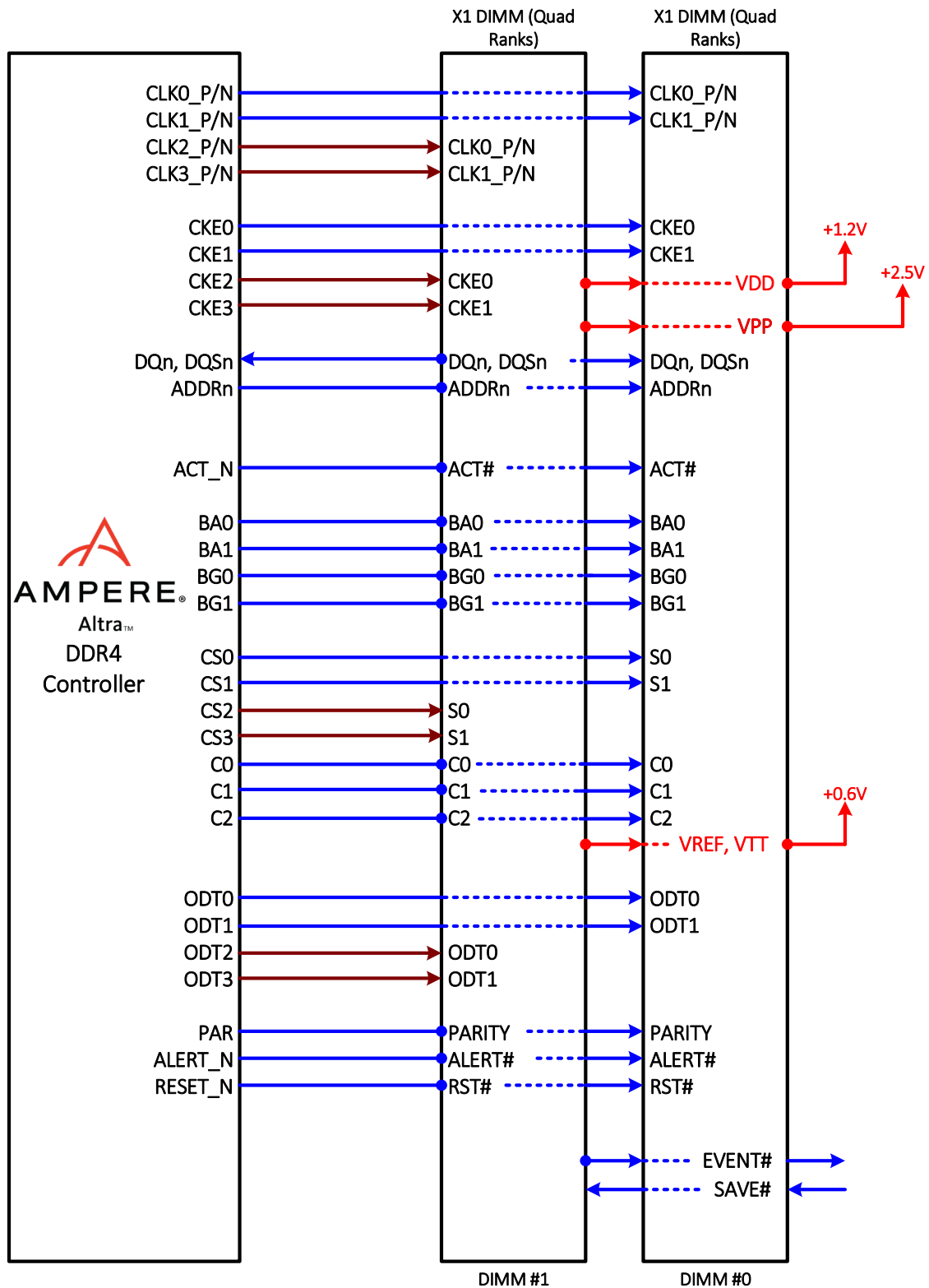




Figure 9: DDR4 Signal Connectivity for Two DIMMs per Channel



Note: DIMM#0 connectivity serves 1DIMM per channel configuration.



2.2.3 DIMM Connectors

- Consider using SMD or through DIMM connectors. SMDs have better performance due to larger spacing and reduced pin stub.
- With 2DPC (two DIMMs per channel) configurations, Slot0 (DIMM0) is the one which is farther from the CPU and Slot1 (DIMM1) is closer to the CPU.

2.3 PCIe/CCIX Subsystem

2.3.1 PCIe/CCIX Ports and Lane Configurations

Altra provides 128 PCIe Gen4 lanes with 48 controllers to support 96 lanes of PCIe and up to 2 x16 Cache Coherent Interconnect for Accelerators (CCIX) links. This capability is based on eight 16-lane multi-port Root Complexes.

There are two types of 16-lane root complexes:

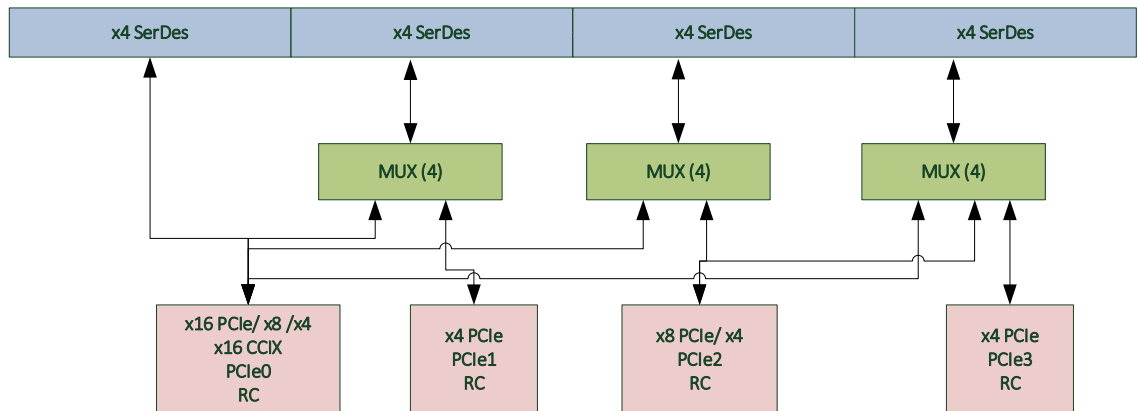
- Type A: Bifurcation from x16 down to four x4s, with a dual-mode x16 PCIe/CCIX controller (refer to [Figure 10](#)).
- Type B: Bifurcation from two x8s down to four x4s.

Altra instantiates 4 Root Complexes of Type A (RcA) and 4 Root Complexes of Type B (RcB).

A Type A Root complex's x16 SerDes supports the following topologies:

- An x16 PCIe interface (by grouping all four x4 SerDes), or
- Two x8 PCIe interfaces (by grouping two contiguous x4 SerDes), or
- One x8 and two x4 PCIe interfaces (by grouping the first two contiguous x4 SerDes or the last two contiguous x4 SerDes), or
- Four x4 PCIe interfaces

Figure 10: Type A Root Complex's x16 SerDes Configuration



A Type B Root complex's x16 SerDes is divided into two identical x8 lanes where each x8 supports the following topologies:

- An x8 PCIe interface (by grouping two x4 SerDes), or
- Two x4 PCIe interfaces



2.3.2 Reference Clock Scheme

Altra takes in a small number of refclks that are used by the various PLLs and SerDes macros in the chip. The following section summarizes these refclks, their usage, and all the aspects of how these are taken in and distributed to all the PLLs and SerDes macros.

There are two defined refclk inputs to Altra:

- SRNS: Separate PCIe reference clock (non-SSC) which is also used for the reference clock for the MCUs, SOC, PCP and all QCPUn PLLs.
- SRIS: Separate PCIe independent reference clock (SSC).

The two reference clocks happen to always be 100 MHz and are PCIe-compliant clocks generated on the board. As such, they are differential HCSL inputs via pairs of package balls and die bumps.

- REFCLK_SRNS is the non-SSC refclk for the multiple PLLs and for the PCIe SerDes. This refclk is always needed and must always be provided.
- REFCLK_SRIS is the SSC refclk for the PCIe SerDes.

There is a refclk-mux (from *Silicon Creations*) that can select between REFCLK_SRNS and REFCLK_SRIS and then drive this refclk to the SerDes.

Refer to the section titled [Clock Distribution](#) for details.



2.3.3 PCIe Reset Scheme

Each agent implements a soft reset (controlled by a register bit) which is similar to a warm reset. The soft reset for an agent only applies to the agent block. For instance, the PCIe controller soft reset resets the controller only.

Altra has a total of 48 PCIe controllers and does not have a dedicated PERST for each controller.

As an alternative solution for PERST per controller, a set of GPIOs (at most 6 GPIOs defined as outputs) are connected to a CPLD which decodes the PCIe reset request and assert the proper reset to the endpoint.

Altra resets each PCIe device by sequence, one device at a time, or resets all devices at the same time.

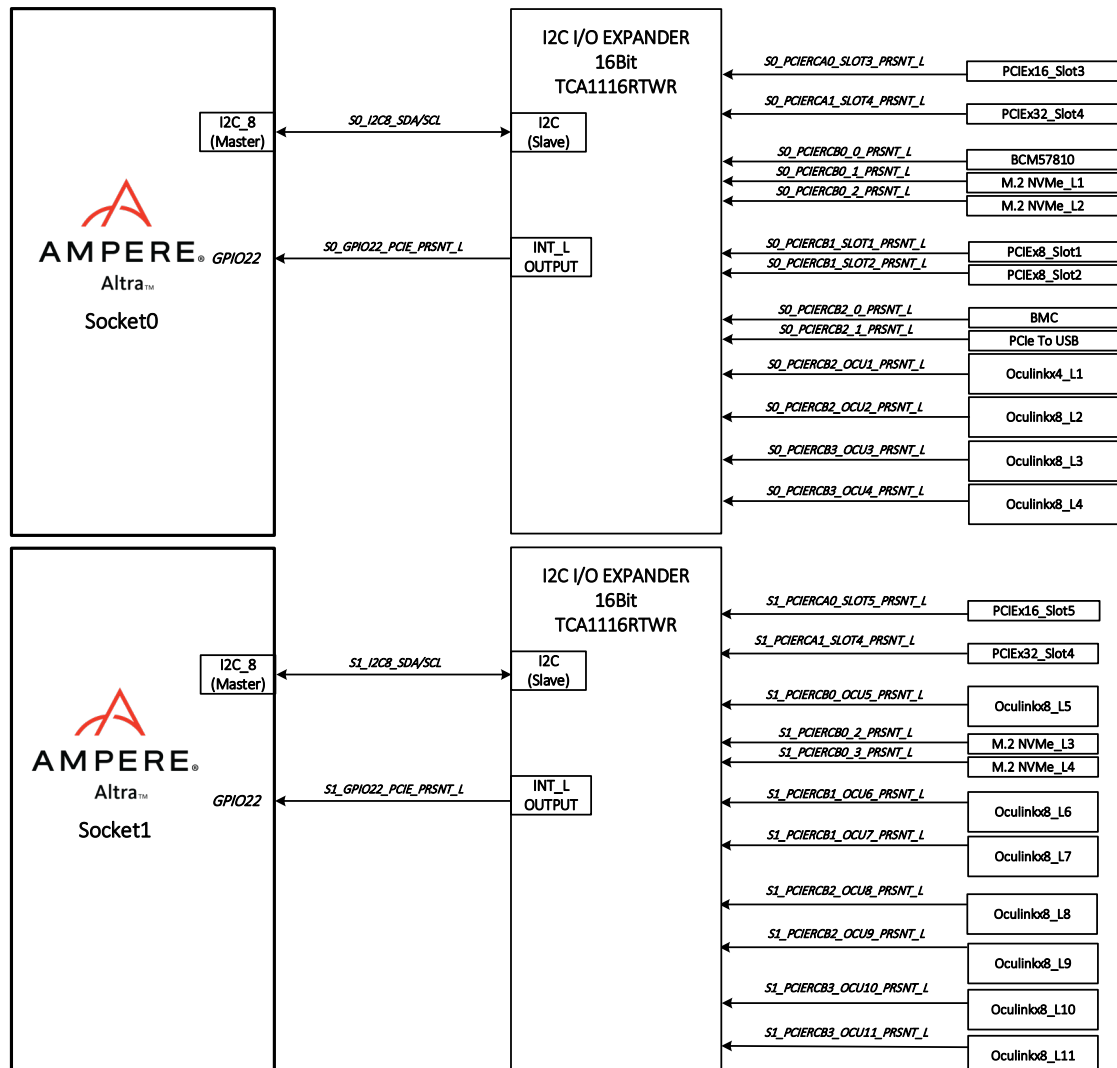
Refer to the section titled [Reset Distribution](#) for details.

2.3.4 PCIe Card Presence Detection

In a real system, there are multiple cards installed. Hence, it may not be possible to use a CPLD to encode or Altra to decode (similar to the reset scheme).

The I2C I/O expander for PCIe Card Detect proposed is shown in [Figure 11](#). On boot-up, software scans the I/O Expander to know which card is present. The I/O expander also supports interrupt output if any I/O pins change level; in this case, GPIO22 is configured as IRQ input.

Figure 11: PCIe Card Presence Detection





2.3.5 PCIe Hot-Plug Support

Altra does not have a native hot-plug controller. Instead, it uses external hot-plug controller and communication is done through I2C or GPIO interface depending on the platform requirements. Refer to [Figure 12](#) and [Figure 13](#) for hot-plug reference connection diagrams.

Figure 12: PCIe Card Hot-Plug Connection Diagram

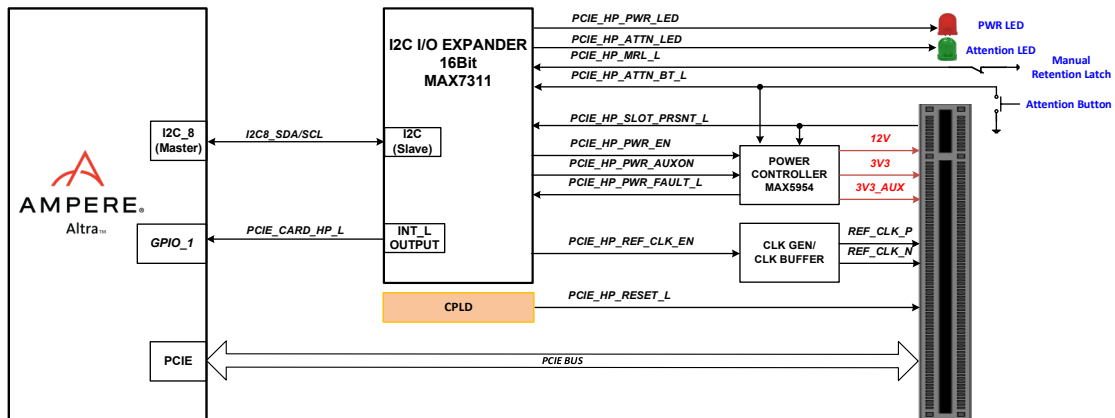
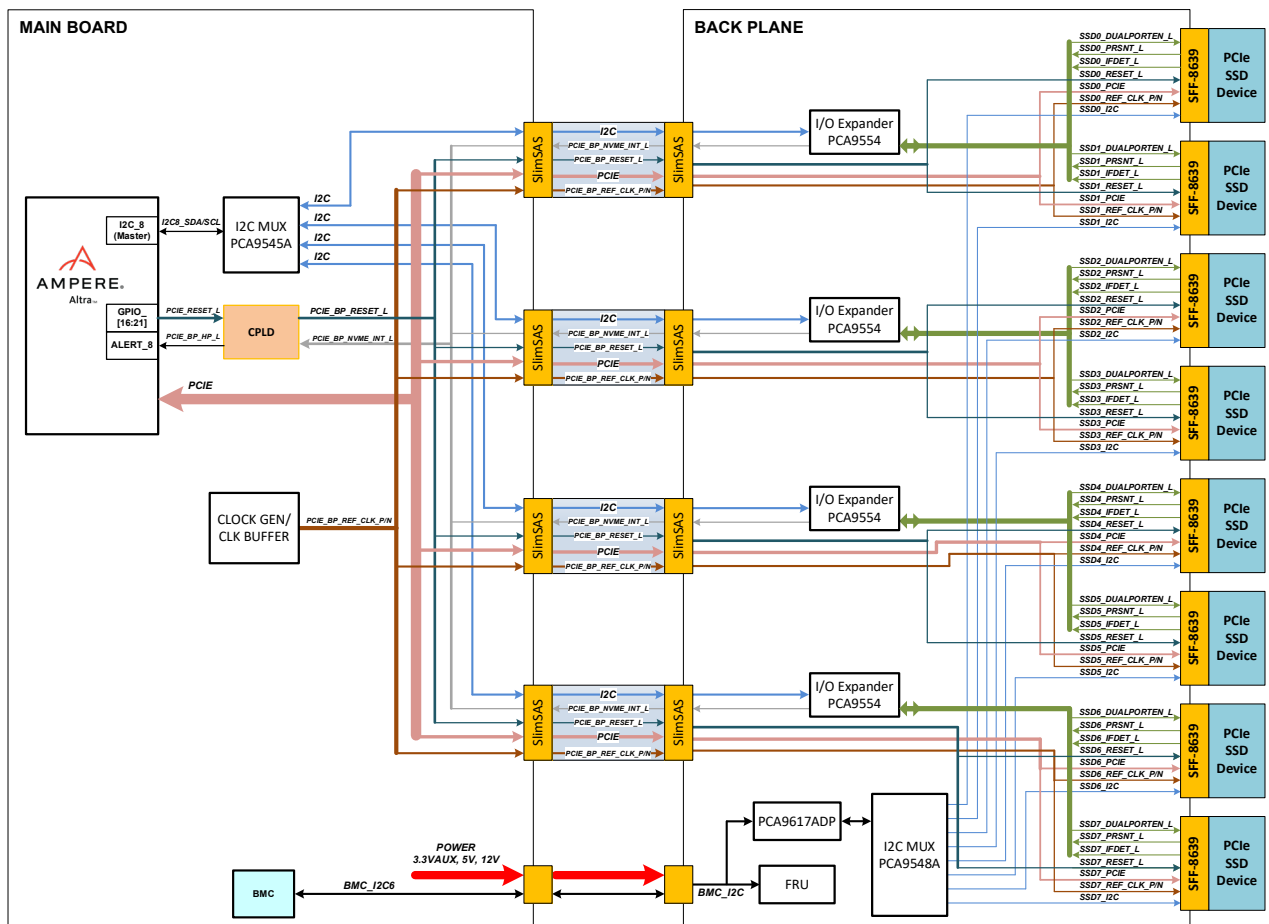


Figure 13: PCIe NVMe SSD Hot-Plug Connection Diagram



Note: Only x4 PCIe controllers support graceful hot-plugging/removal. For details of the hot-plug implementation, refer to the document titled *Altra PCIe Hot-Plug Specification* available on Ampere Computing's Customer Connect portal at <https://connect.amperecomputing.com>.



2.3.6 Schematic Design Guide

2.3.6.1 Power Supply Filtering and Decoupling

2.3.6.1.1 Board Bypass Capacitors

Supply bypass capacitors are recommended to minimize power supply noise. Simulation of the power delivery network is required to determine the actual capacitor values. Depending on their size, each capacitor has a different equivalent series resistance (ESR) and equivalent series inductance (ESL) that determines the capacitor's effectiveness over a frequency range. In general, several low-value capacitors must be placed as close as possible to the package pins. Larger-value capacitors can be placed farther away. Refer to [Table 1](#) for a sample list of the supply bypass capacitors.

Connect the supply bypass capacitors as close as possible to the package pins to ensure a tight return path and maximize their effectiveness. When connecting from the package pin to the bypass capacitors, use as wide a plane as possible to reduce both inductive as well as resistive losses. Typical capacitor placement can be either under the package in the BGA pin field using a low inductance attachment, or closer at the peripheral of BGA on the same side.

The key to get proper PCB decoupling is to have low mounting inductance with proper layout practice, have power plane and closely spaced GND plane for low spread inductance. Capacitor choices are made to suppress resonance in the low/mid frequency range and get as flat and low impedance curve as possible.

Table 1: Example of Supply Bypass Capacitors

COMPONENTS	VALUE
Power supply bypass capacitors	0.01 μ F, 0.1 μ F, 4.7 μ F, 10.0 μ F



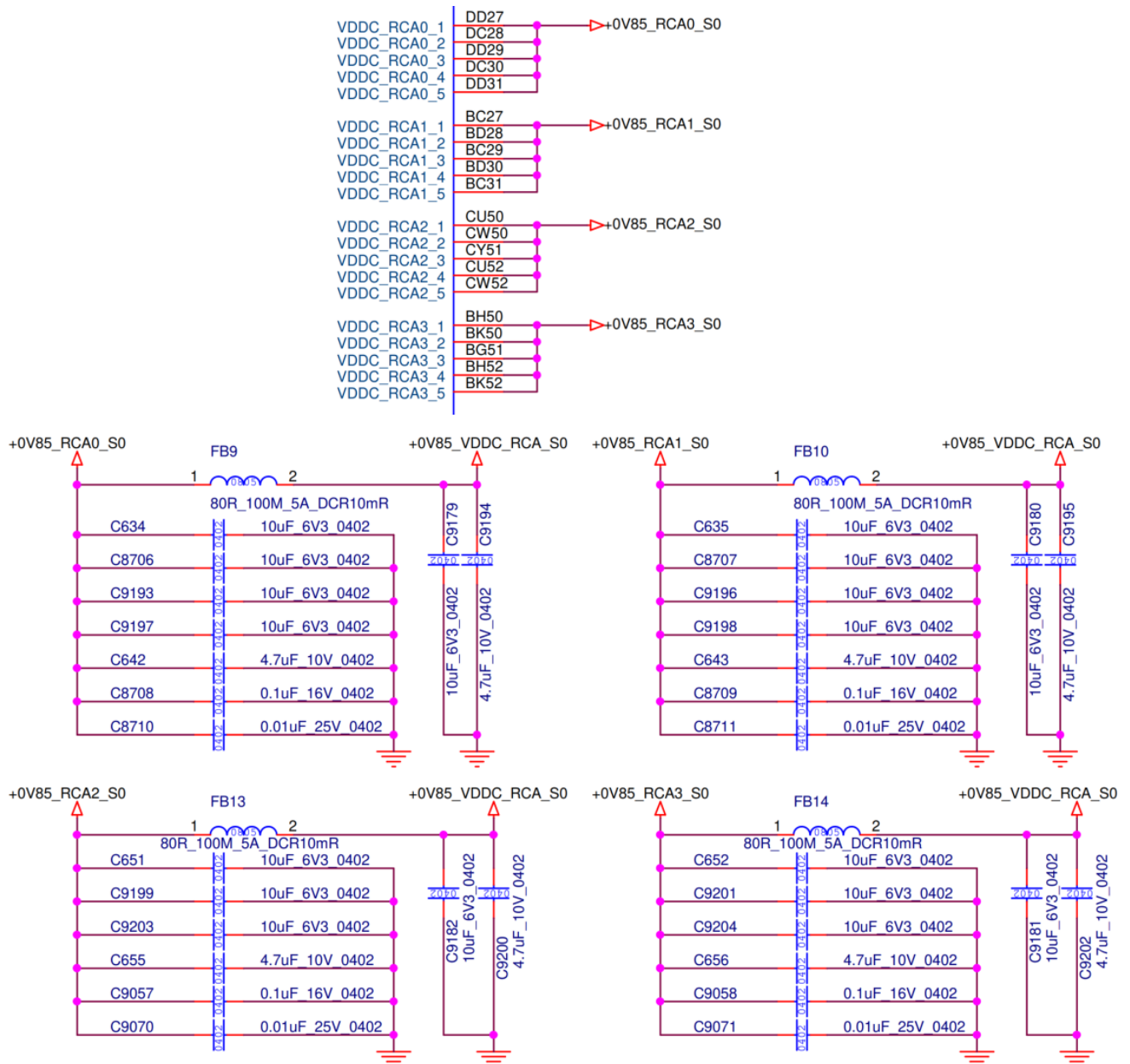
2.3.6.1.2 Ferrite Beads for the Analog Supply Pins

Use a ferrite bead (or inductive choke) to isolate power-supply noise present on each on-board power supply. Power integrity and noise analysis are recommended to determine the correct specification of the ferrite bead to be used.

When using a ferrite bead, put a bulk decoupling capacitor (for example, 10 μ F or 22 μ F) between the package pin and ferrite. This helps the supply current at mid/low frequency as ferrite inductance may limit the current at low end. Select ferrite and decoupling capacitors carefully to ensure noise isolation between the PHY and external noise, and at the same time provide a low-impedance path for transient current demand of PHY. Simulation of decoupling network is highly recommended.

Refer to [Figure 14](#) for an overview of the usage of ferrite beads and decoupling capacitors for analog power pins.

Figure 14: Ferrite Beads and Decoupling Capacitor for Analog Power Pins

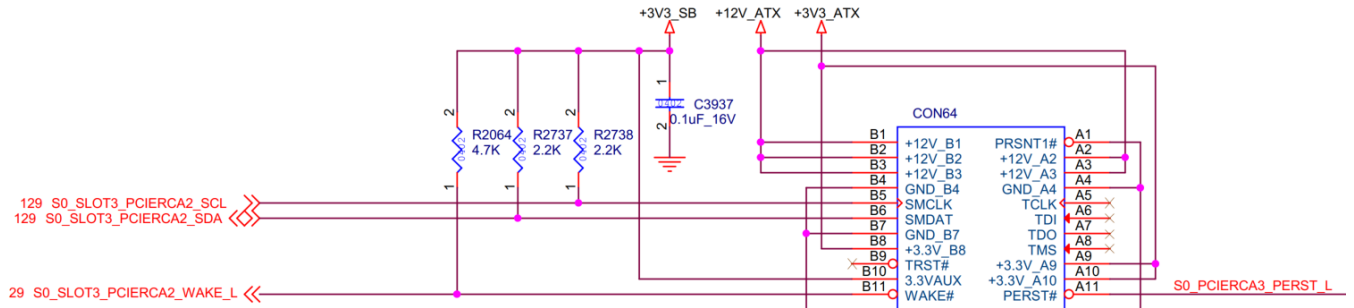




2.3.6.2 PCIe I2C Connection

The PCIe I2C connection must follow [Figure 15](#) in that pull-up resistors of SCL/SDA are connected to pin B10 – 3.3VAUX.

Figure 15: PCIe I2C Connections



2.3.6.3 PCIe Root-Complex Connectivity

[Figure 16](#) shows the PCIe 4.0 Root Complex connectivity on Altra. [Figure 17](#) shows the CCIX connection between two sockets.

Figure 16: PCIe 4.0 Root Complex Connectivity Diagram

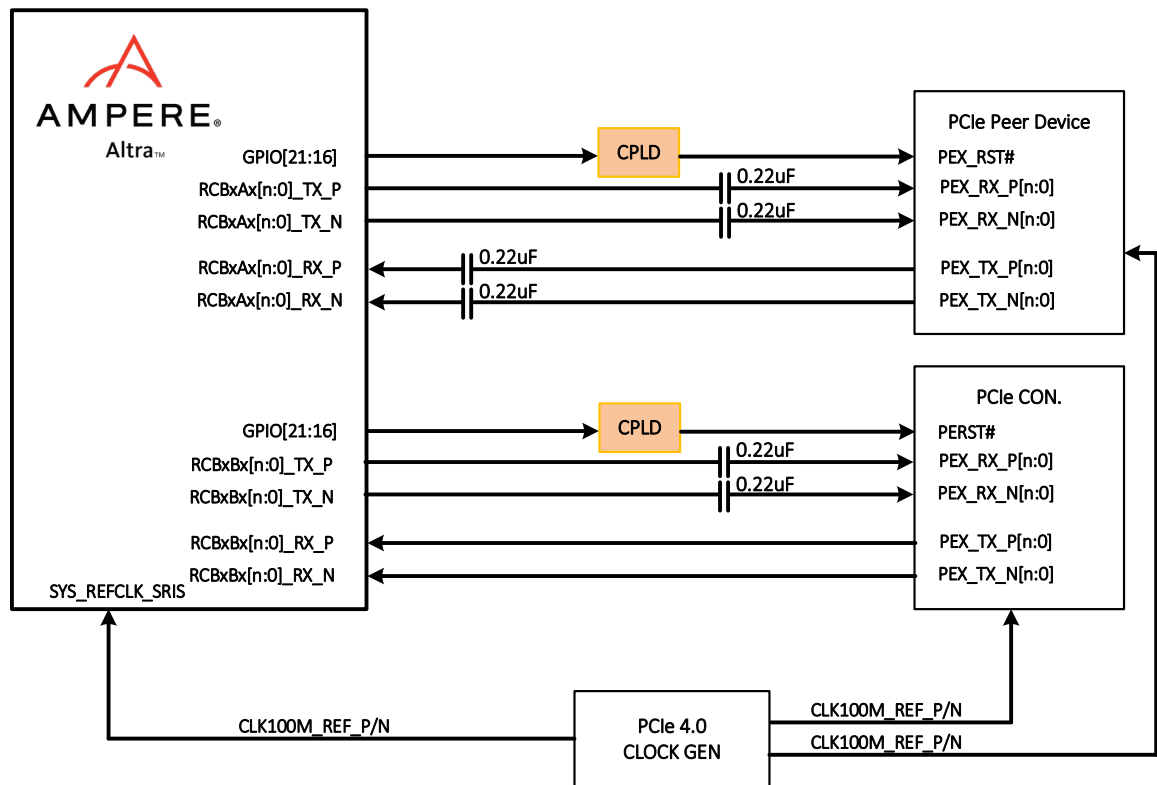
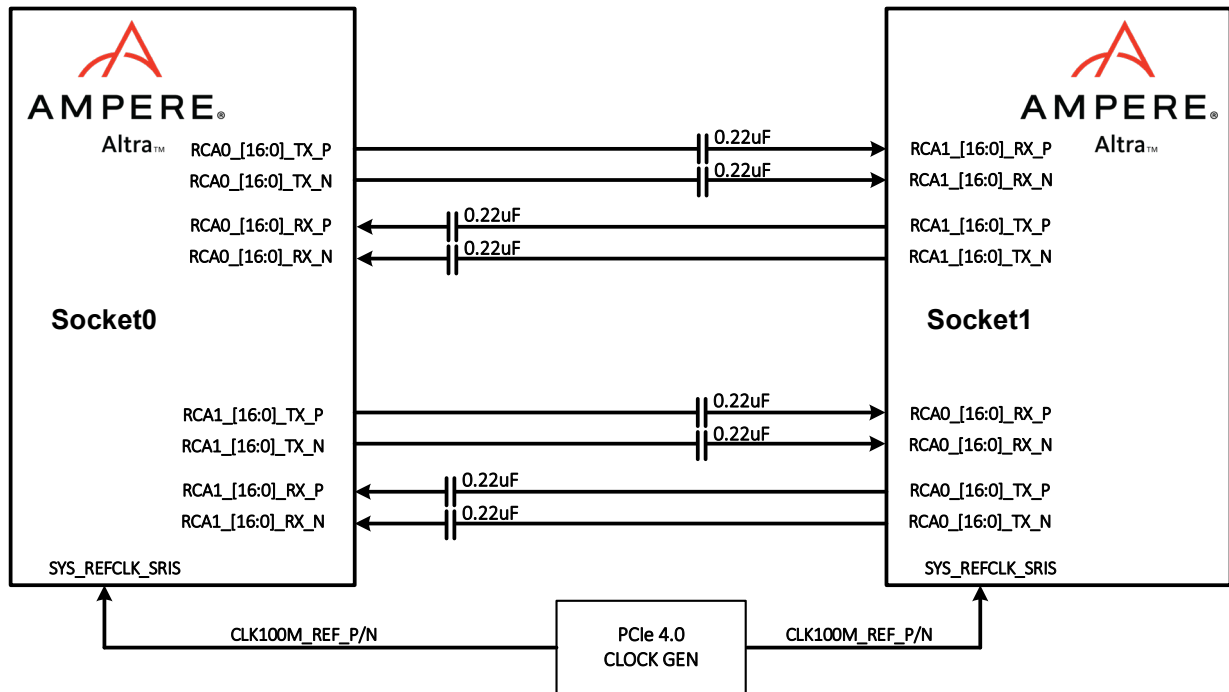




Figure 17: CCIX Connection Between Two Sockets



AC coupling capacitor requirements:

- 2.5/5 GT/s: 75-265 nF
- 8/16 GT/s (Rev 4.0): 176-265 nF
- Requires an X7R 0402 capacitor. Place all AC coupling capacitors on both Tx and Rx if connected to Peer Devices on board and place capacitors on Tx only if connected to PCIe connector.
- The PCIe reference clock source uses PCIe Gen4 clock generator.

2.3.6.4 Termination if Unused: Do Not Connect

2.3.7 Signal Groups

Table 2 lists the signal groups for PCIe Root Complex A and Root Complex B.

Table 2: PCIe Signals

SIGNAL NAME	WIDTH	I/O	I/O TYPE	DESCRIPTION	NOTES
Root Complex Type A (PCIERCA[0:3]): A dual-mode x16 PCIe Gen4/CCIX controller. Altra has 4x RCAs Each RCA can be configured as x16/x8/x4.					
PCIERCA_x_PERSTN	1	O	3.3V	Refer to the section titled Reset Distribution for details	
PCIERCA_[0:3]_L[0:15]_TX_P	16	O	CML	PCle RCAs transmit data (differential signals)	
PCIERCA_[0:3]_L[0:15]_TX_N	16	O	CML		
PCIERCA_[0:3]_L[0:15]_RX_P	16	I	CML		
PCIERCA_[0:3]_L[0:15]_RX_N	16	I	CML		

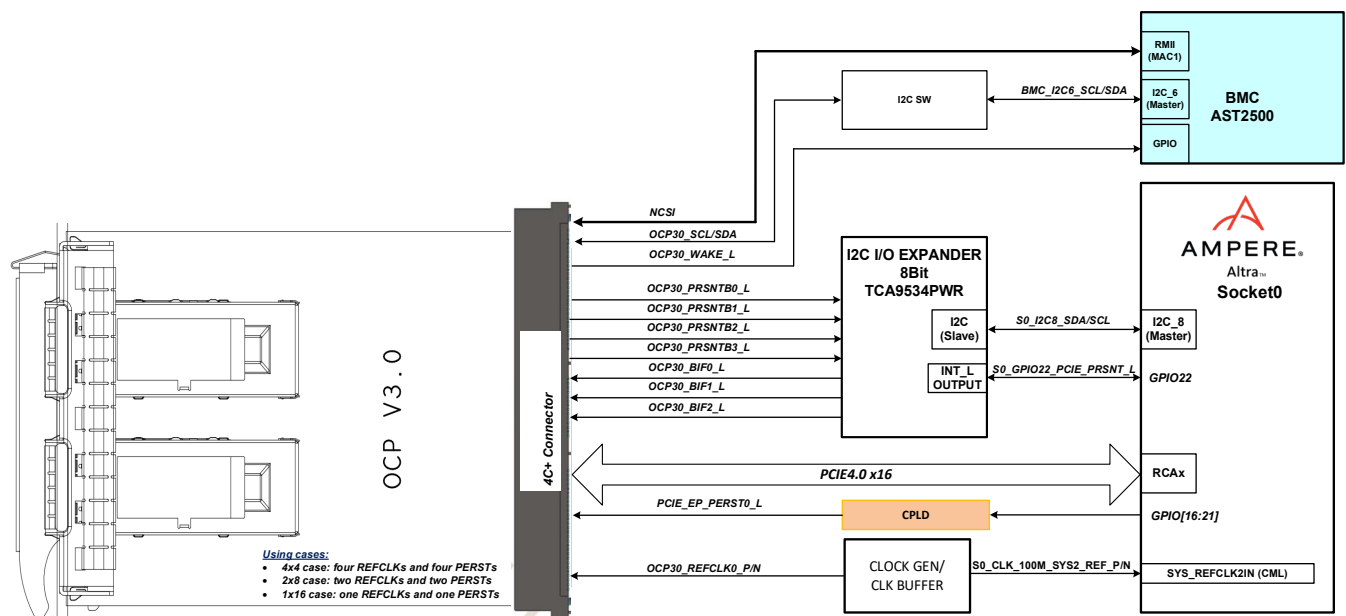


SIGNAL NAME	WIDTH	I/O	I/O TYPE	DESCRIPTION	NOTES
Root Complex Type B (PCIERCB): Altra has 4x RCBs. Each RCB is divided into two identical x8 lanes (RCB does not support x16 lanes) Each RCB can be configured as x8/x4/x2.					
PCIERCB_[0:3]_A_PERSTN	1	O	3.3 V	Refer to the section titled Reset Distribution for details	
PCIERCB_[0:3]_A_L[0:7]_TX_P	16	O	CML	PCIe RCBx A transmit data (differential signals)	
PCIERCB_[0:3]_A_L[0:7]_TX_N	16	O	CML		
PCIERCB_[0:3]_A_L[0:7]_RX_P	16	I	CML	PCIe RCBx A receive data (differential signals)	
PCIERCB_[0:3]_A_L[0:7]_RX_N	16	I	CML		
PCIERCB_[0:3]_B_PERSTN	1	O	3.3 V	Refer to the section titled Reset Distribution for details	
PCIERCB_[0:3]_B_L[0:7]_TX_P	16	O	CML	PCIe RCBx B transmit data (differential signals)	
PCIERCB_[0:3]_B_L[0:7]_TX_N	16	O	CML		
PCIERCB_[0:3]_B_L[0:7]_RX_P	16	I	CML	PCIe RCBx B receive data (differential signals)	
PCIERCB_[0:3]_B_L[0:7]_RX_N	16	I	CML		

2.4 Networking

Figure 18 shows the reference connection diagram of a PCIe x16 OCP NIC 3.0 card configuration. For details and other configurations, refer to the [OCP NIC 3.0 Specification](#).

Figure 18: OCP NIC 3.0 Reference Diagram





2.5 Storage

Figure 19 shows the onboard M.2 NVMe and backplane U.2 NVMe storage reference diagrams.

Figure 19: Onboard M.2 NVMe and Backplane U.2 NVMe

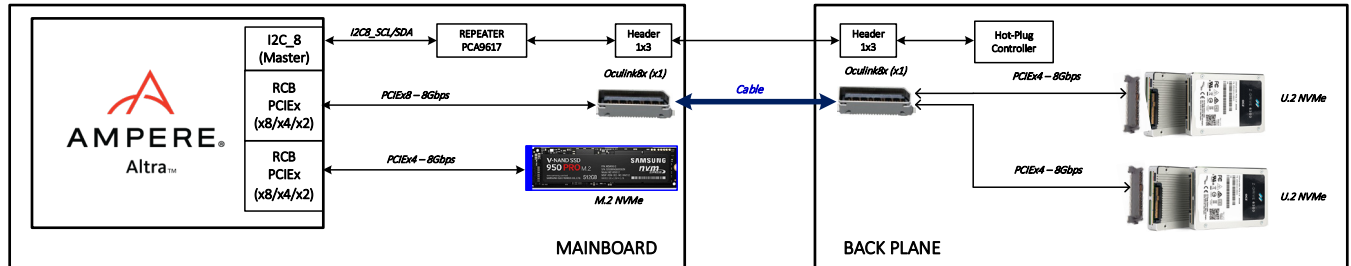
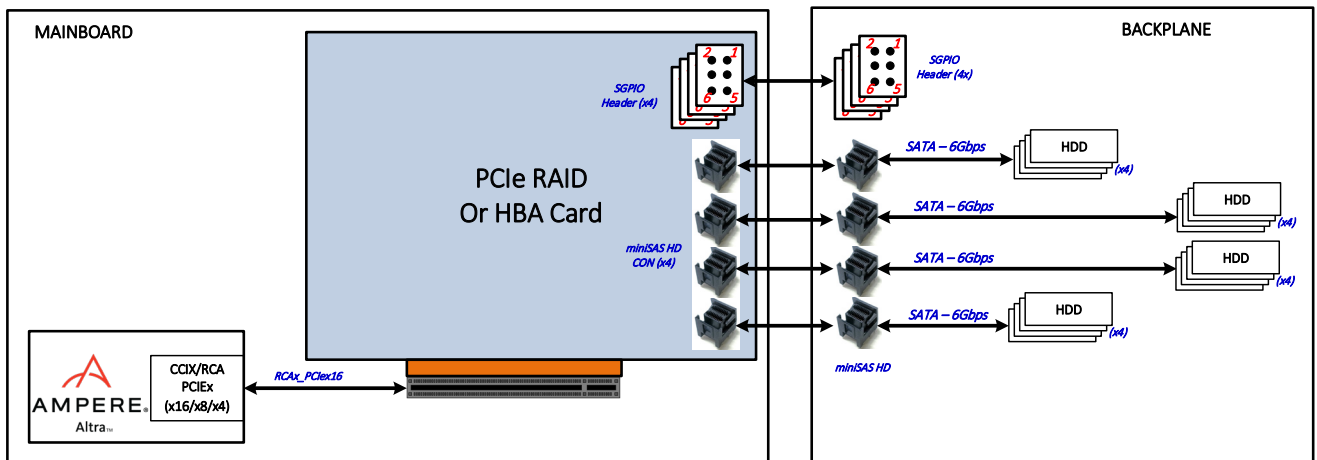


Figure 20 shows the connectivity reference diagrams for HBA card SATA/SAS storage.

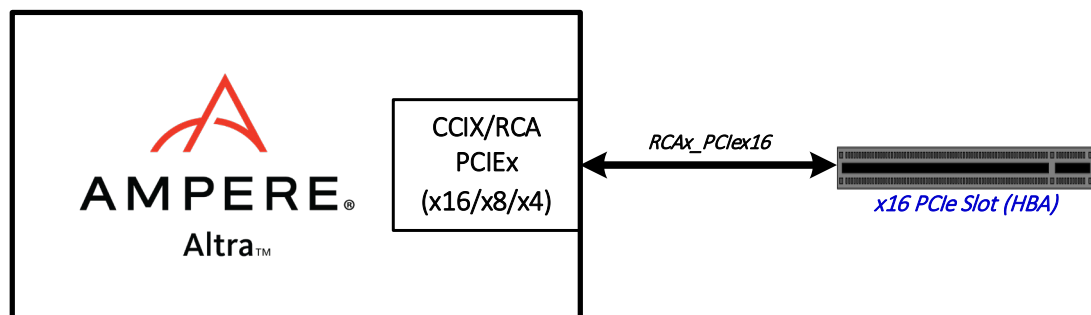
Figure 20: HBA Card Connectivity with Backplane for SAS/SATA Devices



2.6 CCIX Acceleration

Figure 21 shows the CCIX implementation using a x16 PCIe link.

Figure 21: CCIX Implementation using PCIe x16 Ports





3. Management Subsystem

The primary functions of Altra server board management subsystem are:

- IPMI 2.0 support for remote management
- IPMB support for chassis management
- System power control
- System Event Log
- Sensor monitoring (e.g. voltage, temperature, fans, PSU)
- Fan control (fail detection, speed control)
- Serial Over Lan
- Asset Information (FRU)
- Auto recovery from hang (Watchdog)
- Remote KVM and Media

The Altra server board uses ASPEED AST2500 as the Baseboard Management Controller (BMC). The BMC subsystem hardware configuration is listed in [Table 3](#).

Table 3: BMC Functions

INTERFACES	CONFIGURATION
Memory	512 MB DDR4 memory with ECC support
PCIe	• VGA support • x1 PCIe Gen2, configured as EP, direct connection to Altra socket0 PCIe port RCB2A
VGA	1 VGA port with 1920x1028 resolution
SPI	• A 512 Mb main flash for BMC boot • A 512 Mb failover flash for BMC boot
I2C	• Two I2C ports (I2C3/I2C1: Master/Slave) for Altra in-band/out-of-band communication • One I2C port (I2C2) to access system boot EEPROM • One I2C port (I2C4) for current, temperature monitoring, FRU access • One I2C port (I2C5) for RTC access • One I2C port (I2C6) for PCIe sideband signals • One I2C port (I2C7) for PSU access • One I2C port (I2C8) for Backplane PWR control
eMMC	• One 4 GB eMMC connector to SD2 bus
ETH	• One 1 GE RGMII port • One 100 M RMII port (NCSI)
UART	• One 4-pin UART port • Three 2-pin UART ports • One 2-pin UART for BMC console
USB	• One USB port, directly connected to PCIe-USB bridge chip • One USB port connects to HDR1x4
GPIO	Refer to Table 6 for GPIO pin assignments
ADC	Monitors all power rails of motherboard
PWM/TACH	Supports 6 fan controllers

3.1 Baseboard Management Controller (BMC)

AST2500 is the sixth generation of Integrated Remote Management Processor from ASPEED Technology Inc. It is a vastly integrated SOC device playing as a service processor to support various functions required for highly manageable server platforms. Instead of supporting PCI bus, AST2500 is designed to dedicatedly support PCIe Gen2 x1 bus interface, which can make PCB layout simpler and fit systems that are going without PCI bus support.

Figure 22: BMC Functional Diagram



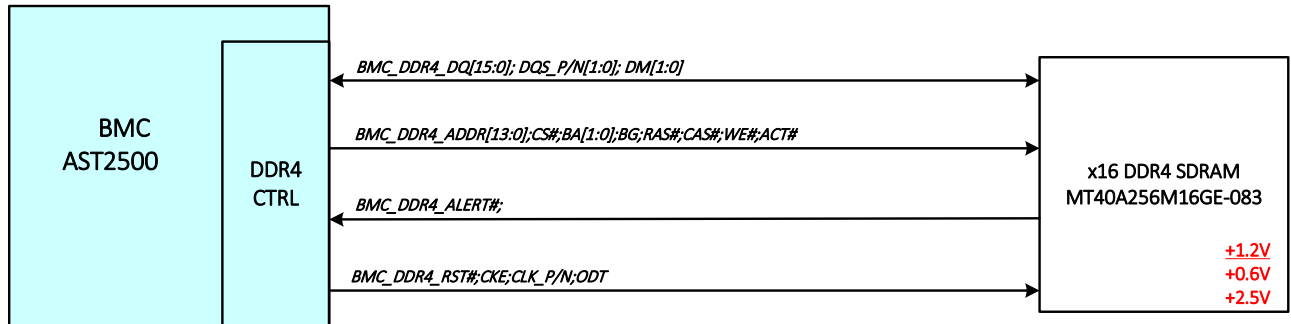


3.1.2 BMC Features on Altra

AST2500 is configured on the Altra board to support the interfaces described in the following subsections.

3.1.2.1 DDR4 Memory

Figure 23: BMC DDR4 SDRAM Block Diagram

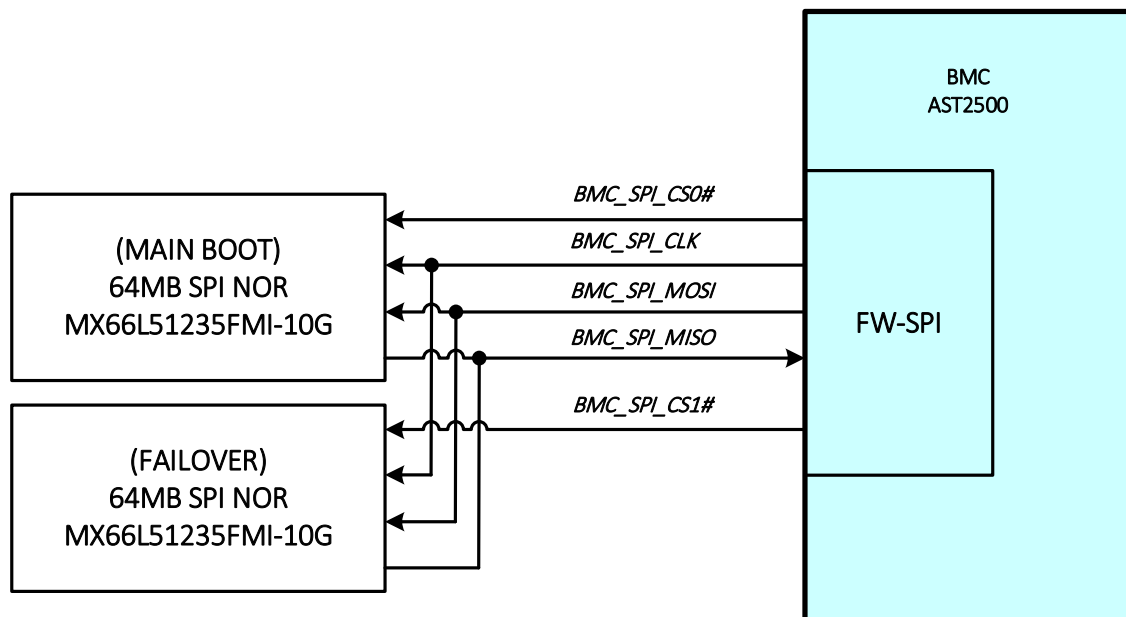


- Support for external 16-bit DDR4 SDRAM data bus width, maximum clock frequency 800 MHz (DDR4 1600 Mbps).
- Only supports the DRAM size that has Column address (CA) = 10 bits (A0~A9).
- Support for DDR4 DRAM types: 128 MB x 16, 256 MB x 16 (MT40A256M16), 512 MB x 16.
- Only supports DRAM Burst Length = 8 modes.
- Integrated DDR I/O PHY with automatic timing and driving calibration capability.
- Support for programmable size ECC protection function, with an overhead of memory size equal to 1/8 ECC protected memory size.
- For additional information, refer to the latest *AST2500/AST2520 Application Design Guide, Version 1.4*.

3.1.2.2 Serial Peripheral Interface (SPI)

Figure 24 shows how to connect BMC's SPI to SPI buses of two sockets.

Figure 24: BMC SPI Diagram



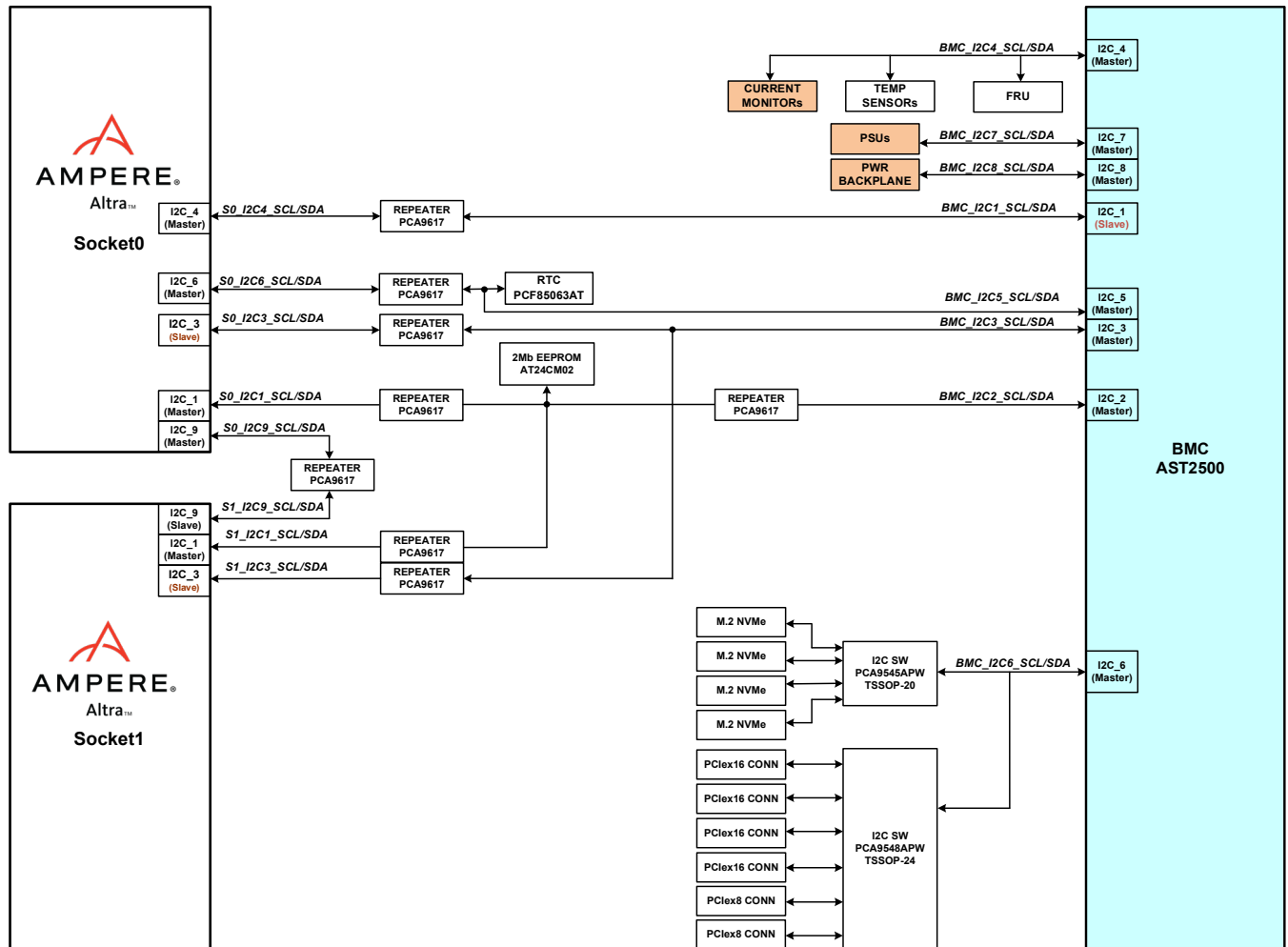
There are two SPI NORs (recommended part number: MX25L2573FMI-10G) for BMC firmware, supporting the second-boot firmware failover function. The system automatically reboots from the second flash connected to chip select SPI_CS1# if the main flash connected to chip select SPI_CS0# does not boot up successfully.



3.1.2.3 I2C Networks

Figure 25 shows the BMC's I2C connection in detail.

Figure 25: BMC I2C Network



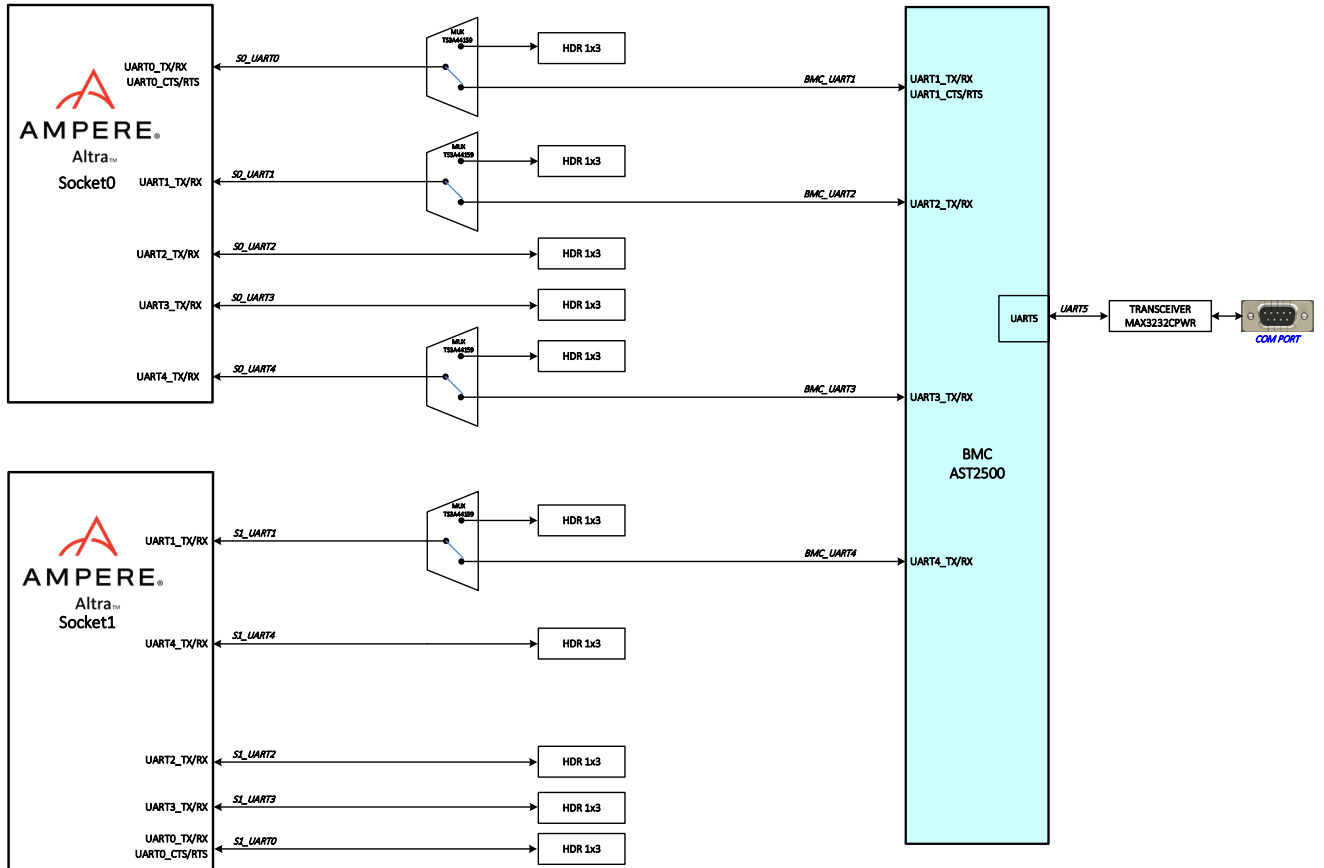
This system employs 8 x I2C buses of BMC to manage the board:

- I2C1 (Slave): BMC receives Socket0's IPMI SSIF requests
- I2C2 (Master): Two Altra sockets boot from one EEPROM. This I2C bus allows BMC to update the boot image.
- I2C3 (Master): As a master I2C, BMC requests to both sockets' I2C slave.
- I2C4 (Master): Current monitors, temperature sensors and FRU EEPROM
- I2C5 (Master): RTC
- I2C6 (Master): M.2 NVMe and PCIe connectors
- I2C7 (Master): PSU
- I2C8 (Master): Backplane power



3.1.2.4 UARTs

Figure 26: UART Connection Diagram



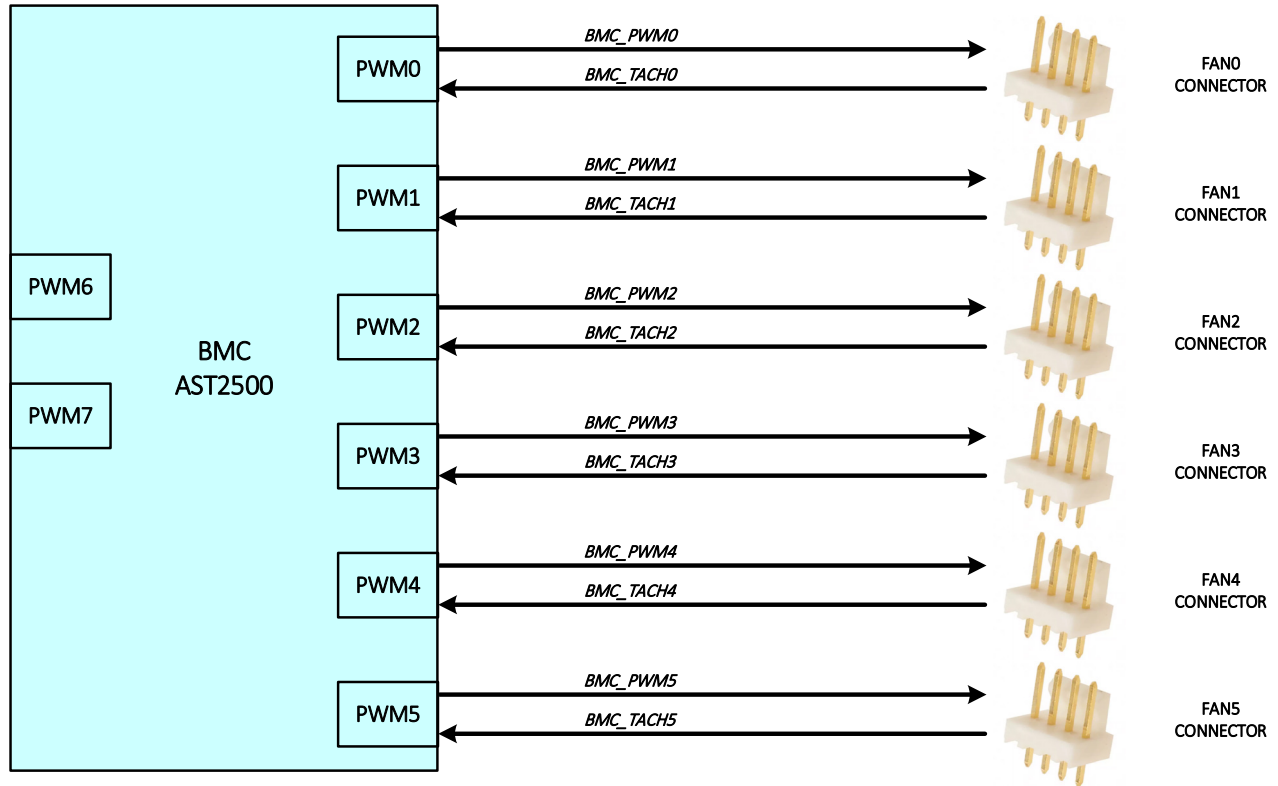
In this system, BMC supports 5 UART ports, with up to 115.2K baud rate:

- One 4-pin UART (UART1): Connects to Socket0's UART0 to support UEFI and OS console Serial-over-LAN (SoL).
- One 2-pin UART (UART2): Connects to Socket0's UART1 to support SMpro console Serial-over-LAN.
- One 2-pin UART (UART3): Connects to Socket0's UART4 to support ATF console Serial-over-LAN.
- One 2-pin UART (UART4): Connects to Socket1's UART1 to support SMpro console Serial-over-LAN.
- One 2-pin UART (UART5) is BMC console.



3.1.2.5 PWM/TACH for Controlling and Monitoring Fans

Figure 27: BMC Fan Control and Monitor



BMC AST2500 supports 8 PWMs to controls fans. The Altra platform uses 6 PWM[0:5]; PWM[6:7] are reserved. Each fan can have a different speed under firmware control and based on environmental inputs. The initial duty cycle is set up by firmware. Fan connectors used for the Altra platform are the 4-pin type. Based on design requirements, the connector can be changed. The fan's RPM is monitored from TACH[0:5] inputs.

3.1.2.5.1 PWM Controller

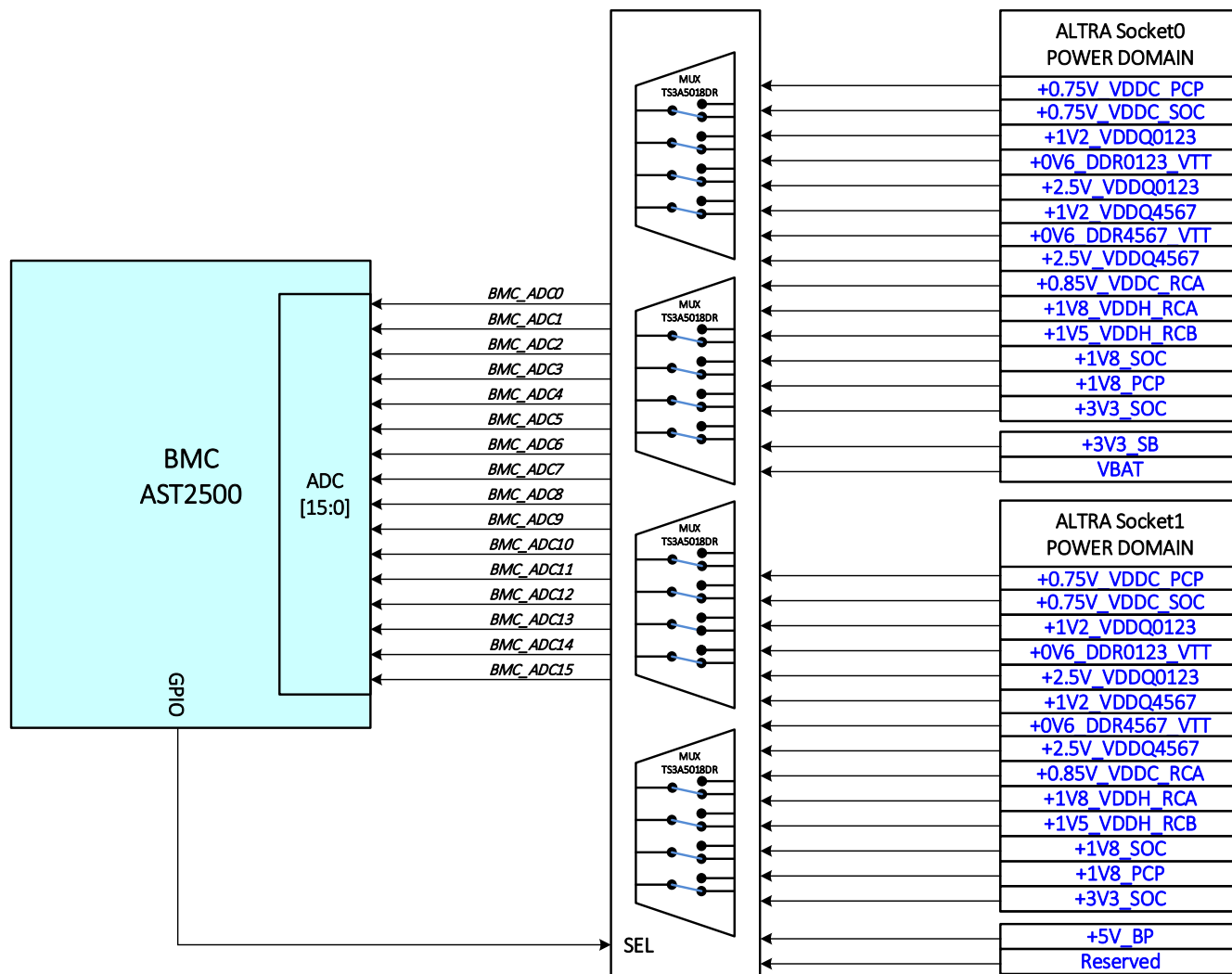
- Support for a maximum of 8 PWM outputs
- Supports 3 types of frequency mode PWM for fan speed control
- Duty cycle from 0 to 100% with 1/256 resolution
- Support for low-frequency PWM pulse stretching for fan speed measurements

3.1.2.5.2 Fan Tachometer Controller

- Support for 6 tachometer inputs
- Measurement schemes: rising edge, falling edge or both edges
- Supports interrupt trigger when fan overspeed limitation setting is enabled

3.1.2.6 ADC for Voltage Monitors

Figure 28: BMC Power Rails Monitor



The BMC AST2500 monitors voltage levels for the power supplies on the Altra platform. ADC inputs can only accept voltage range between 0V and 1.8V. For a higher input voltage for measurement, it must be divided by a resistor divider. A better input voltage for monitoring is $\frac{3}{4}$ of the maximum voltage, which is about 1.35V. BMC AST2500 has maximum 16 ADC channels. Hence, for a dual-socket platform, a 2:1 mux is recommended to select which power rail needs to be monitored.

Because the BMC's maximum ADC range is 1.8 V, it is recommended using a voltage divider for the power rails listed below:

- Power rails 0 – 1.5 V: Use a divider in the ratio 1:1
- Power rails 1.8 V – 2.5 V: Use a divider in the ratio 1:2
- Power rail 3.3 V: Use a divider in the ratio 1:3
- Power rail 5 V: Use a divider in the ratio 1:4



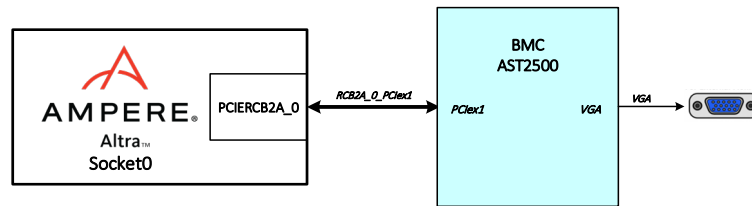
3.1.2.7 PCIe for VGA

Socket0's PCIe RCB2A is connected to BMC AST2500's PCIe x1 Lane with Gen2 for supporting VGA function.

Features:

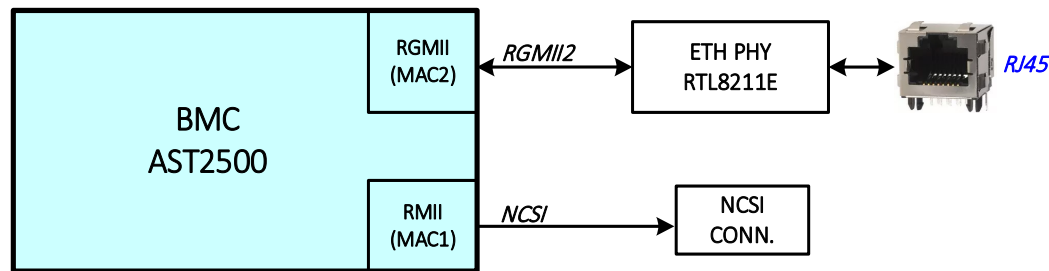
- Fully IBM VGA compliant
- Maximum display resolution: 1920x1200 @ 60 Hz with 165 MHz video clock
- Integrated one dedicated PLL for video clock generation which can be directly turned off by Altra for power saving
- Support for 64x64 hardware overlay cursor with both mono and color formats

Figure 29: BMC VGA Display Port



3.1.2.8 Network Interfaces

Figure 30: BMC Network Interfaces



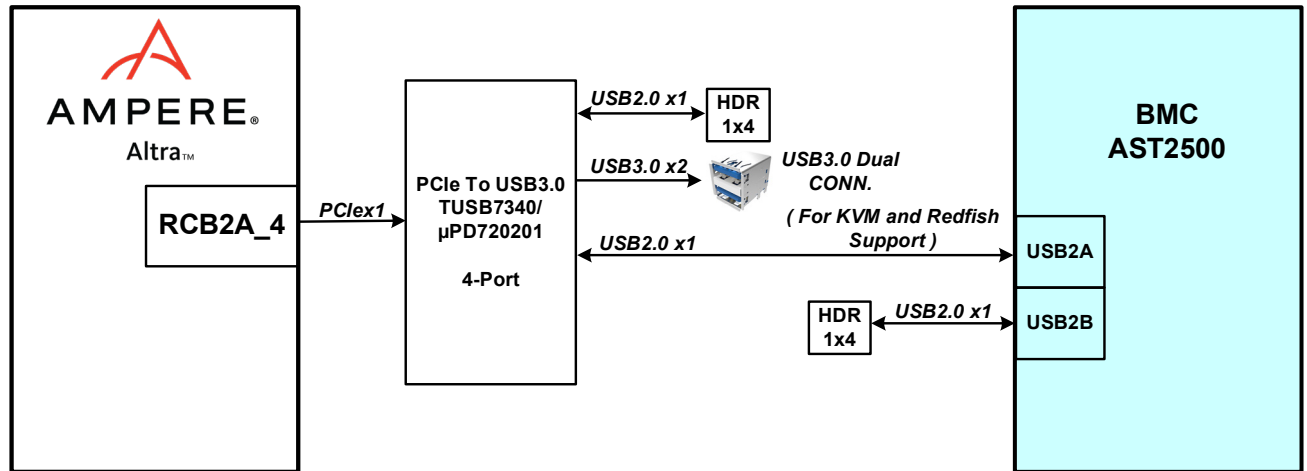
- BMC has 2 integrated MACs compliant with IEEE 802.3 and IEEE 802.3z specification
- Support for half- and full-duplex (1000 Mbps mode only supports full duplex)
- Supports flow control for full-duplex and backpressure for half-duplex
- BMC's MAC2 is connected to 1 GbE PHY to manage server
 - Supports 10/100/1000 Mbps transfer rates
 - Supports Reduced Gigabit Media Independent Interface (RGMII)
 - An RJ45 connector located at the front of the server provides 1 GbE connectivity to an external management switch
 - The PHY must be Realtek RTL8211E or equivalent.
- BMC's MAC1 is connected to NCSI connector
 - When using NCSI function, firmware needs to handle the handshake with NCSI controller
 - It can connect to OCP card through NCSI connector to support out of band function.

For reference design, refer to *Section 4.3: Pin Function Configuration* and *Section 15: 10/100/1000M Ethernet MAC Interface* in *AST2500 Application Design Guide – V1.4*.



3.1.2.9 USB Interfaces

Figure 31: BMC USB Interfaces



- BMC's USB2A supports USB 2.0 Virtual Hub Controller
 - Compliant with USB Specification Revision 2.0
 - Supports USB 2.0 standard and is backward compatible with USB 1.1 standard
 - Supports one hub port and 5 downstream ports with configurable endpoint types
 - Supports USB, KVM, and Redfish over LAN architecture
 - Connected to Altra's PCIe RCB2A port through external PCIe to USB device TUSB7340
- BMC's USB2B is configured as USB 2.0 Host Controller:
 - Compliant with USB Specification Revision 2.0
 - Supports Low/Full/ High-speed mode transfers
 - Connected to Header 1x4

For reference design, refer to *Section 4.3: Pin Function Configuration* and *Section 16: USB Interface* in *AST2500 Application Design Guide – V1.4*.

Refer to [Figure 32](#). BMC supports a JTAG master controller. Any JTAG Slave can be programmed through this JTAG port. The board must contain mux circuitry controlled by the BMC to switch the BMC to the three programming paths: CPLD, Altra's JTAGs and PCIe_JTAG. Note that there still must be a CPLD JTAG Header for a backup plan to use external CPLD programming tool to program CPLD. Refer to [Table 4](#) for JTAG control signal descriptions.

Figure 32: BMC JTAG Master Programming Diagram



SIGNAL NAME	DESCRIPTION
CPU_JTAG_DSCHN_DIS_BMC_GPIO	Output from BMC/Jumper to CPLD and CPU This signal disables internal daisy-chaining of the JTAG DAPs (IPP, PM and DAP). High = The DAPs are routed to the 3 individual JTAG ports. Low = All 3 DAPs are daisy chained on the main DAP JTAG port.
SLAVE_PRESENT_N	Input to BMC and CPLD from Slave CPU This signal indicates to CPLD and BMC that CPU was mounted on S1. High = The CPU is not on S1. Low = The CPU was mounted on S1.
BMC_CON1_SEL_BMC_GPIO	Output from BMC/Jumper to CPLD This signal is used to select BMC or CON1 for JTAG master debugging. High = Select BMC for JTAG master debugging. Low = Select CON1 for JTAG master debugging.



Table 5: JTAG Mode Selection

JTAG ACCESS MODE	CPU_JTAG_DSYCHN_DIS_BMC_GPIO	SLAVE_PRESENT_N	BMC_CON1_SEL_BMC_GPIO	DESCRIPTION
Option 1 with Debugger access: – System has S0 only – CON1 access to S0 internal daisy chain – CON2 access to S0 SOC JTAG	0	1	0	CON1: => S0, JTAG DAP->IPP->PM (CPU internal daisy chain) CON2 => S0, JTAG SOC
Option 1 with BMC JTAG access: – System has S0 only – BMC access to S0 internal daisy chain – CON2 access to S0 SOC JTAG	0	1	1	BMC: => S0, JTAG DAP->IPP->PM (CPU internal daisy chain) CON2 => S0, JTAG SOC
Option 2 with Debugger access: – System has S0 and S1 – CON1 access to both S0 and S1 internal daisy chain – CON2 access to both S0 and S1 SOC JTAG	0	0	0	CON1: => S0 JTAG DAP->IPP->PM => S1 JTAG DAP->IPP-PM (CPU internal daisy chain) CON2 => S0 JTAG SOC => S1 JTAG SOC
Option 2 with BMC JTAG access: – System has S0 and S1 – BMC access to both S0 and S1 internal daisy chain – CON2 access to both S0 and S1 SOC JTAG	0	0	1	BMC: => S0 JTAG DAP->IPP->PM => S1 JTAG DAP->IPP-PM (CPU internal daisy chain) CON2 => S0 JTAG SOC => S1 JTAG SOC
Option 3 with Debugger access: – System has S0 only – CON1 access to S0 DAP JTAG – CON3 access to S0 IPP JTAG – CON4 access to S0 PM JTAG – CON2 access to S0 SOC JTAG	1	1	0	CON1 => S0, JTAG DAP CON3 => S0, JTAG IPP CON4 => S0, JTAG PM CON2 => S0, JTAG SOC



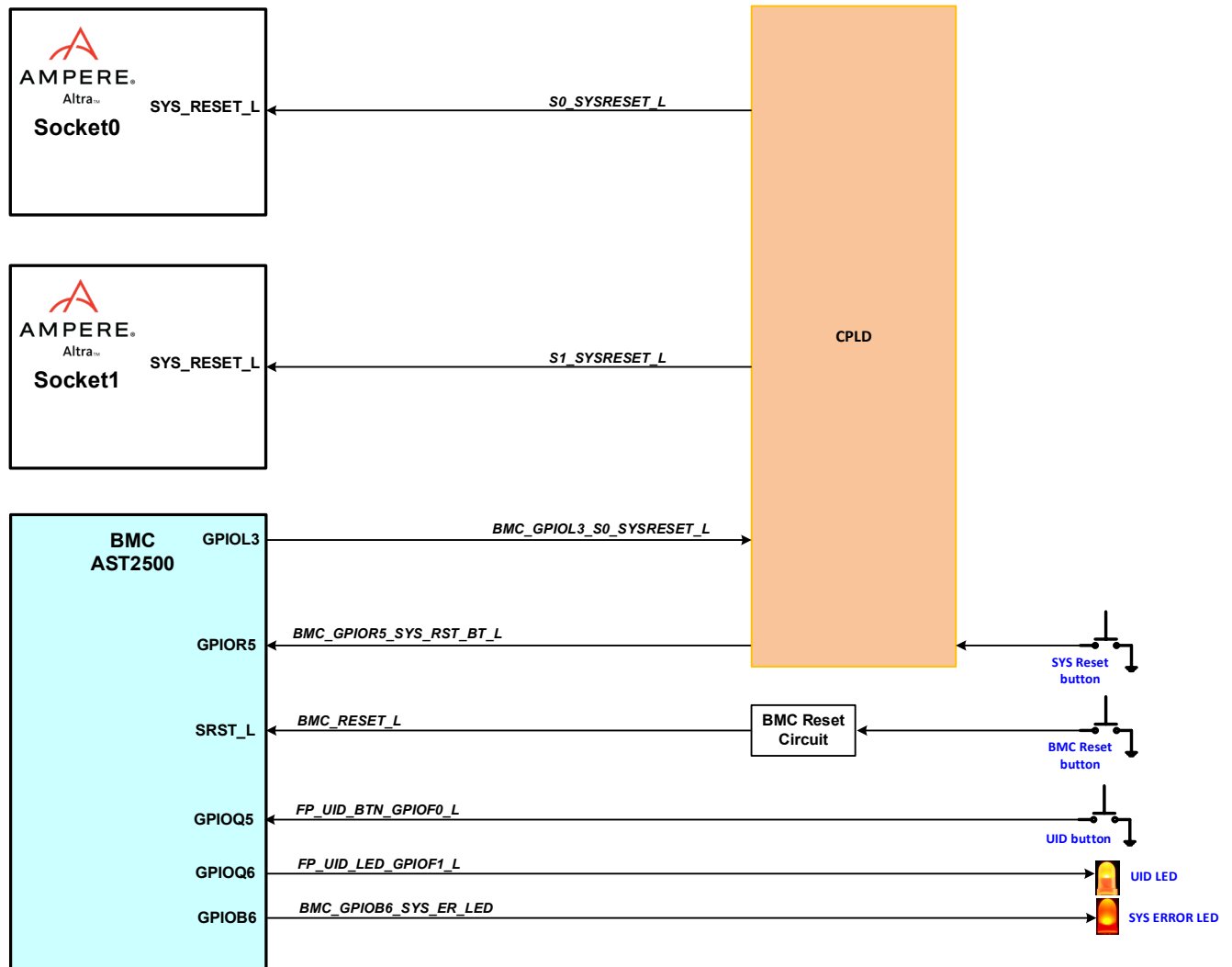
JTAG ACCESS MODE	CPU_JTAG_DSYCHN _DIS_BMC_GPIO	SLAVE_PRESENT_N	BMC_CON1_SEL_ BMC_GPIO	DESCRIPTION
Option 3 with BMC JTAG access: – System has S0 only – BMC access to S0 DAP JTAG – CON3 access to S0 IPP JTAG – CON4 access to S0 PM JTAG – CON2 access to S0 SOC JTAG	1	1	1	BMC => S0, JTAG DAP CON3 => S0, JTAG IPP CON4 => S0, JTAG PM CON2 => S0, JTAG SOC
Option 4 with Debugger access: – System has S0 and S1 – CON1 access to both S0 and S1 external daisy chain on platform – CON2 access to both S0 and S1 SOC JTAG external daisy chain on platform	1	0	0	CON1: => S0 JTAG DAP->IPP->PM => S1 JTAG DAP->IPP->PM (external daisy chain in CPLD) CON2 => S0 JTAG SOC => S1 JTAG SOC
Option 4 with BMC JTAG access: – System has S0 and S1 – BMC access to both S0 and S1 external daisy chain on platform – CON2 access to both S0 and S1 SOC JTAG external daisy chain on platform	1	0	1	BMC: => S0 JTAG DAP->IPP->PM => S1 JTAG DAP->IPP->PM (external daisy chain in CPLD) CON2 => S0 JTAG SOC => S1 JTAG SOC



3.1.2.11 User Indicator LEDs

Figure 33 shows the buttons and LED indicators for grabbing the user's attention.

Figure 33: User Indicator LEDs



- Power button: Used to turn on/off the mainboard power. Besides, BMC can also turn on/off the mainboard.
- Sys Reset button: Used to perform a cold reboot of the mainboard (note that this has no effect on the BMC; it only indicates to the BMC that system was reset by the user).
- BMC reset button: Resets only the BMC, does not have any effect on the mainboard.
- UID button and LED: When user presses the UID button, the UID LED turns on to indicate the location of the system on the Server's Rack.
- SYS error LED: This LED turns on upon a system error.
- BMC Boot OK LED: Indicates that BMC is ready.



3.2 I/O Interfaces Between Two Sockets and BMC

[Table 6](#) lists the GPIO interfaces between the two sockets and BMC.

Table 6: GPIO Interfaces Between Two Sockets and BMC

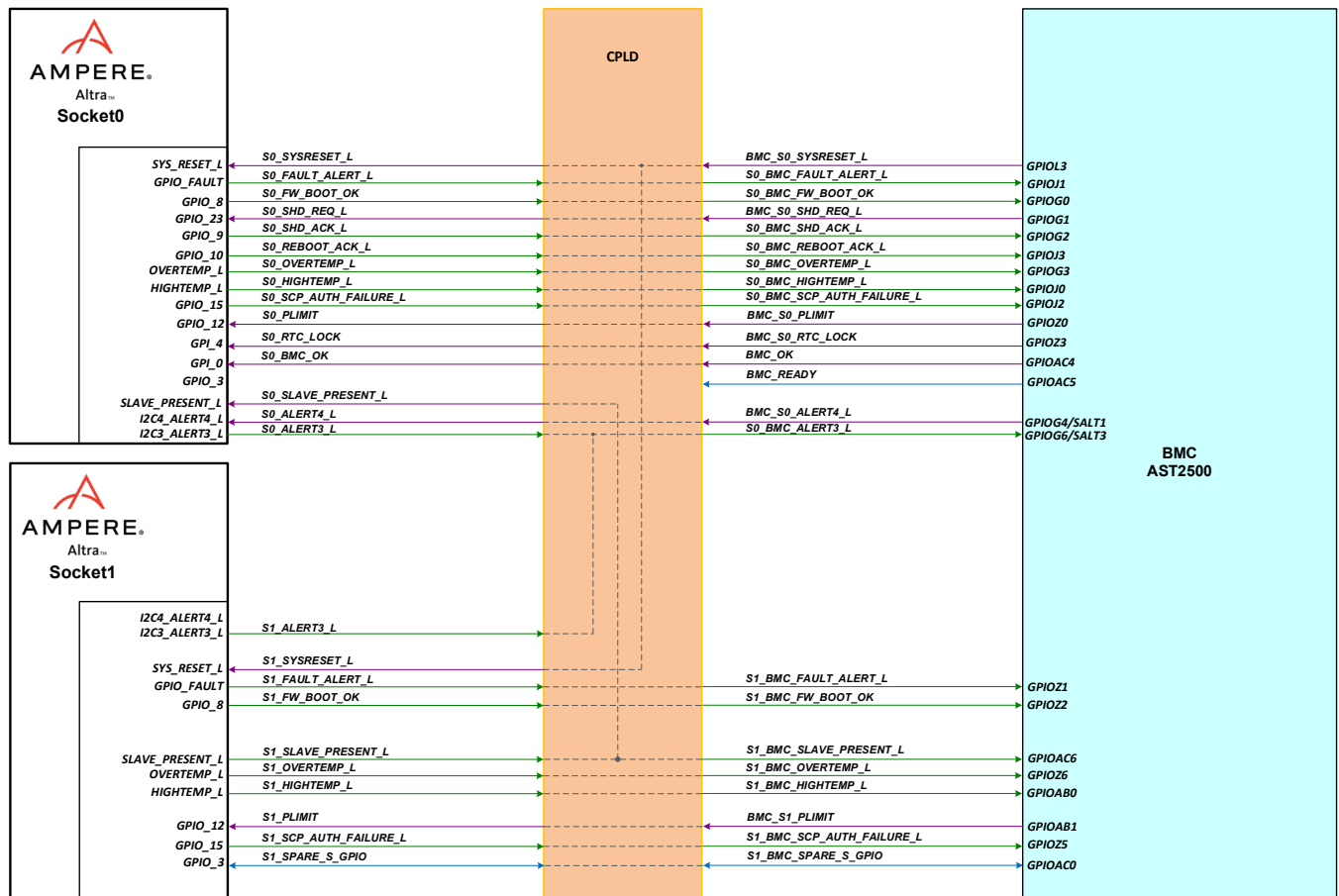
MNEMONICS	SIGNAL	DIR FROM Altra	SOCKET0	SOCKET1	COMMENTS
FW_BOOT_OK	S-GPIO	OUT	Yes	Yes	Set by the host to inform the BMC of the host is in ready status: HIGH if the host is in ready status.
SHD_REQ_L	S-GPIO	IN	Yes	N/A	The input to host from BMC to request a “graceful shutdown”, LOW level triggered.
SHD_ACK_L	S-GPIO	OUT	Yes	N/A	The output from host to BMC. Asserted LOW to acknowledge shutdown request from BMC. Altra also asserts this when it completes a soft shutdown request from the OS.
REBOOT_ACK_L	S-GPIO	OUT	Yes	N/A	The output from host to BMC. Asserted LOW to notify BMC that software reboot executed from OS.
OVERTEMP_L	OVERTEMP	OUT	Yes	Yes	Output LOW from host to BMC to indicate an OVERTEMP event. The OVERTEMP event causes a power off sequence for the entire SoC to be initiated.
HIGHTEMP_L	HIGHTEMP	Bi-Di	Yes	Yes	At boot, this is configured as an input. At internal high temperature, this is configured as an output to BMC. On BMC’s detection of high temperature, asserted by BMC.
SCP_AUTH_FAILURE_L	S-GPIO	OUT	Yes	Yes	The output from host to BMC. Asserted LOW to notify BMC that Secureboot authentication failure
RST_L	SYS_RESET	IN	Yes	Yes	The input to host from the BMC or Reset Push button. Asserted LOW to reset host.
I2C3_ALERT_L	ALERT	OUT	Yes	N/A	The output LOW from host to BMC to notify the BMC of an event on the I2C slave bus.
I2C4_ALERT_L	ALERT	IN	Yes	Yes	LOW level-triggered from BMC to host to notify the host of an event on the SSIF interface.
BMC_OK	S-GPIO	IN	Yes	NA	BMC triggers HIGH level to notify host that it’s ready to receive SSIF messages.



MNEMONICS	SIGNAL	DIR FROM Altra	SOCKET0	SOCKET1	COMMENTS
PLIMIT	S-GPIO	IN	Yes	Yes	BMC drives the signal HIGH to trigger host throttle to the lowest frequency/voltage
SPARE_S_GPIO	S-GPIO	IN/OUT	Yes	Yes	Reserved for future use - recommendation is to connect to BMC
FAULT_ALERT_L	GPIO_FAULT	OUT	Yes	Yes	HIGH level-triggered from host to notify BMC that CPU has a fault/non-recoverable error.
SLAVE_PRESENT_L	SLAVE_PRESENT_L	IN/OUT	Yes	Yes	In the 1P system, this signal is not connected to BMC. In the 2P system, this signal is connected to a BMC and an Altra Master Socket GPIO inputs. It indicates that a Host Slave Socket is present.
RTC_LOCK	GPI	IN	Yes	NA	This signal indicates to Altra that the RTC access is temporarily restricted. BMC drives this signal HIGH to indicate that it needs access to the RTC.
SPARE_S_GPIO	S-GPIO	IN/OUT	NA	Yes	Reserved for future use – recommendation is to connect to BMC



Figure 34: I/O Interfaces Between Two Sockets and BMC



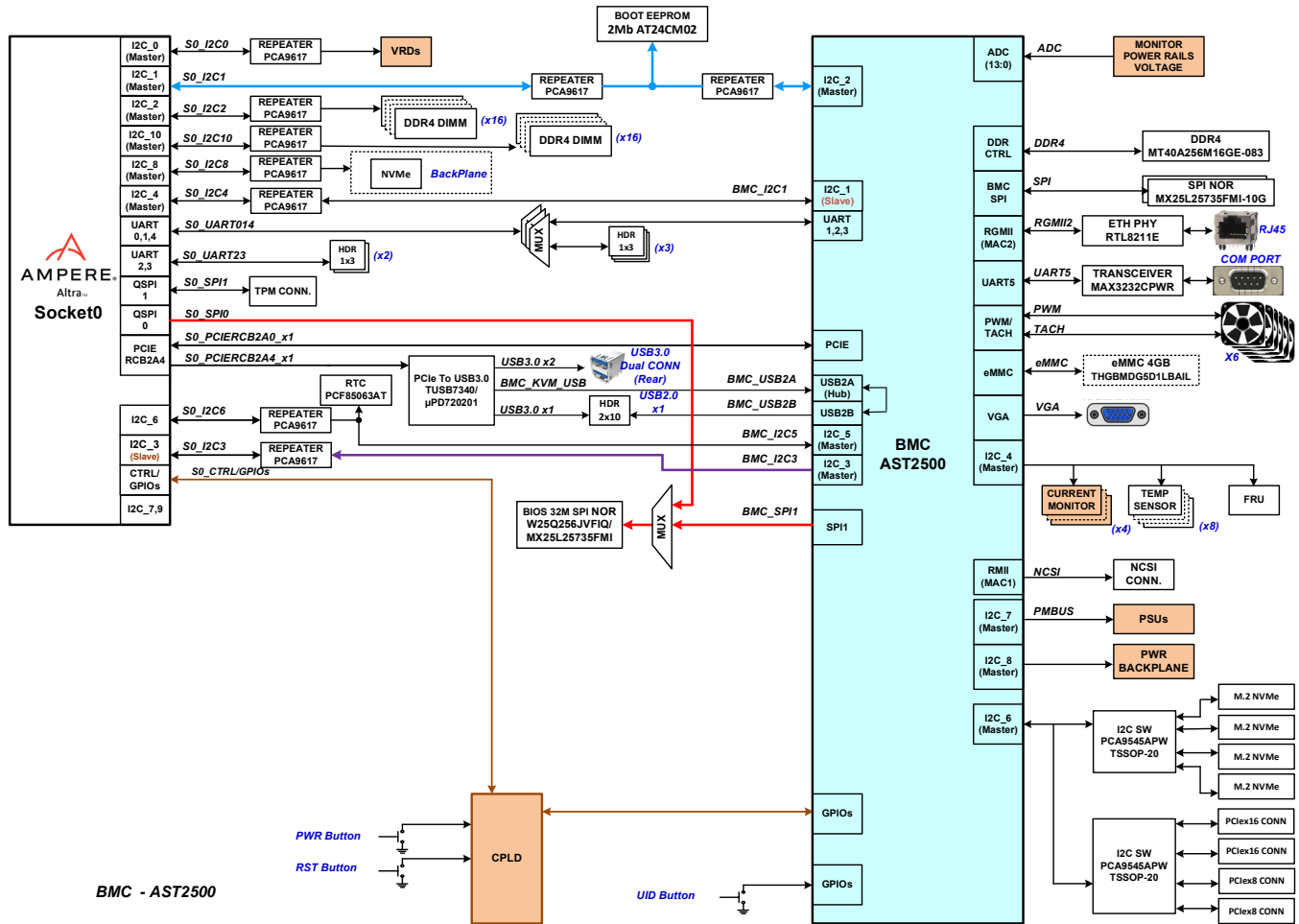


3.3 BMC on Dual-Socket (2P) Systems

Refer to [Figure 22](#) for details.

3.4 BMC on Single-Socket (1P) Systems

Figure 35: AST2500 BMC Block Diagram for Single-socket Platforms





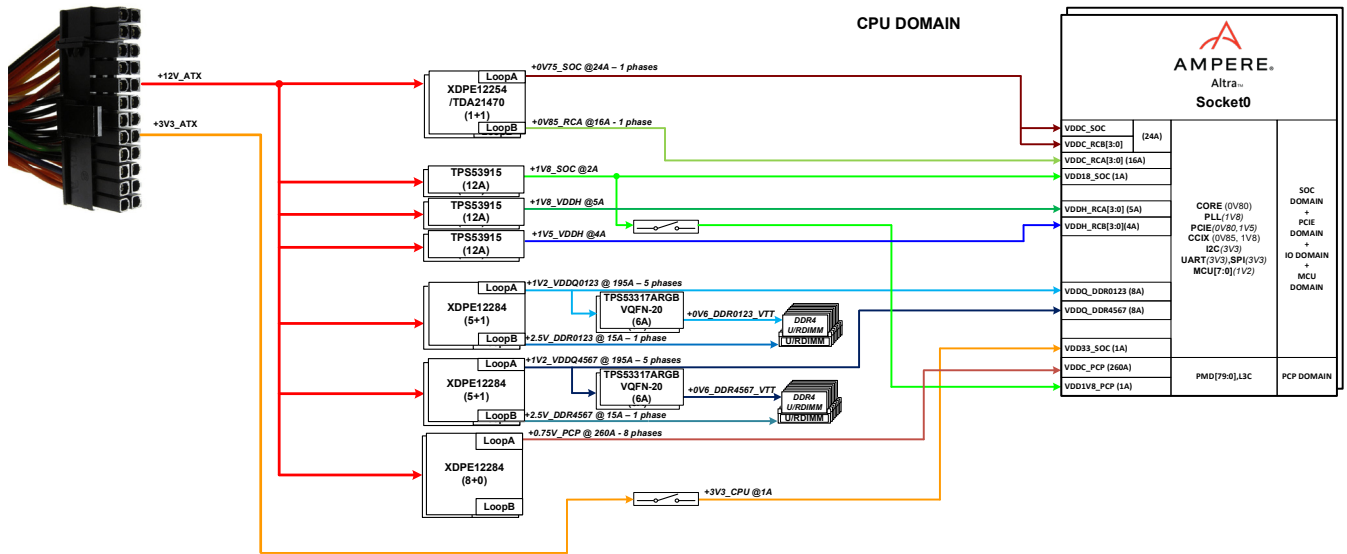
4. Power Supply Design Guidelines

4.1 Power Supply Design Requirements

4.1.1 Physical Design

Altra requires the power rails shown in [Figure 36](#).

Figure 36: Altra Power Supply Diagram



For power rails design requirement, refer to [Table 7](#). Based on this table, the VR for the design can be selected. For details of the VR design guideline, contact the VR vendor.

VRD's phase count: For the VDDC_PCP power rail, the maximum current is up to 300 A, and hence it is recommended selecting an 8-Phase VRD to keep the individual phase currents below 40 A. Less than 8-Phase designs result in TDC current levels that incur power loss through the inductors and FETs which are difficult to manage.

Table 7: Power Rails Design

POWER RAIL	Vin (V)	Vout (V)	Iout_max (A)	# of PHASES (n)	FSW (kHz)	NOTES
VDDC_PCP	12	0.75 – 1.1	300	8	600	For PDN simulations, it is recommended to use 1 V for VDDC_PCP.
VDDC_SOC, VDDC_RCB[0:3]	12	0.75	26.67	1	600	–
VDDC_RCA[0:3]	12	0.85	16	1	600	–
VDDH_RCB[0:3]	12	1.5	4	–	–	Small Regulator
VDDH_RCA[0:3]	12	1.5/1.8	5	–	–	Small Regulator
VDDQ_DDR0123	12	1.2	195	5	600	CPU (10 A) + 8x 256 GB DIMMs (M393ABG40M52)
VDDQ_DDR4567	12	1.2	195	5	600	CPU (10 A) + 8x 256 GB DIMMs (M393ABG40M52)



4.1.1.1 CPU Voltage Identification

The processor sets the voltage regulator to a nominal Voltage Identification set point (VID) at power on reset. Each processor may, at manufacturing time, be produced with unique VID values even within the same SKU (including speed grade). The range of possible VID values that must be supported by the VR, as well as corresponding DC and AC tolerances around the nominal set point, is specified in the section titled [Min/Max Voltages for I/O Power Rails](#). Power supply current load is specified in the section titled [Voltage Regulator Power Efficiency](#).

The VID value for a given processor is provided with a resolution of 1 mV. The system designer must account for quantization errors in conversion from the provided VID value to the VID code table of the selected VR, in order to ensure that the voltage is within the specified DC tolerance range.

Notes:

- The VR must be connected to the I2C0 port. Firmware provides the conversion from the provided VID value to the VID code table of the selected VR. Consult the AVL for a list of currently supported VRs.
- VR must support a default (boot) VID of 750 mV (for VDDC_PCP) and 750 mV (for VDDC_SOC).

4.1.1.2 PCP Voltage

- Min to Max voltage based on AVS table (Overshoot/Undershoot control requirement) is (Nominal – 1%) to (Nominal +1%) with Nominal VR set point = 0.75 – 1.1 V.
- Power Profile Impedance:

The designer needs to design PCB decoupling capacitor network that keeps its impedance under the target impedance up to effective frequency. The target impedance Z_{target} is defined using the maximum allowable voltage ripple and transient current and is provided as follows:

- Reference voltage: 1.0 V
- Total PDN Margin % / mV: 5% / 50 mV @ 1 V
- DC Resistance Target: 0.2 mΩ
- Z_{target} (up to 1 MHz): 0.3 mΩ
- Z_{target} (1 MHz to 10 MHz): 0.4 mΩ

At low frequencies, the VR has very low impedance and is capable of responding to the instantaneous current requirements up to approximately 70 kHz. At higher frequencies, the VR impedance is primarily inductive, making it incapable of meeting the transient current requirement and the decoupling capacitors on boards are used for reducing the impedance profile. As frequency increases to 10 MHz or above, the PCB decoupling capacitors become less effective and on-package decoupling capacitors and on-die-capacitance with lower ESR and ESL should handle this requirement.

4.1.1.3 SoC Voltage

- Min/Max voltage (Overshoot/Undershoot control requirement) is 0.675 V to 0.825 V (Nominal VR set point = 0.75 V).
- Power Profile Impedance:
 - Reference voltage: 0.75 V
 - Total PDN Margin % / mV: 5% / 37.5 mV @ 0.75 V
 - Z_{target} (up to 1 MHz): 2 mΩ
 - Z_{target} (1 MHz to 10 MHz): 5 mΩ

4.1.1.4 SerDes

- Altra supports 2 groups of SerDes, namely RCA (supports up to 25 Gbps) and RCB (support up to 16 Gbps). They require two power supplies VDDC and VDDH for each SerDes. Refer to the section titled [Min/Max Voltages for I/O Power Rails](#) for the minimum and maximum voltage values for the I/O power rails.
- For VDDC_RCA (0.85 V), Min/Max voltage (Overshoot/Undershoot control requirement) is 0.765 V to 0.935 V (Nominal VR Set point = 0.85 V).



- Power Profile Impedance (with 10 mΩ DC-R Ferrite Bead for filtering):
 - Reference voltage: 0.85 V
 - Total PDN Margin % / mV: 5% / 42.5 mV @ 0.85 V
 - Z_{target} (up to 1 MHz): 500 mΩ
 - Z_{target} (1 MHz to 10 MHz): 120 mΩ

4.1.1.5 DDR Voltage

- +1V2_VDDQ0123 and +1V2_VDDQ4567: Min/Max voltage (Overshoot/Undershoot control requirement) is 1.14 V to 1.26 V (Nominal VR Set point = 1.20 V).
- Power Profile Impedance:
 - Reference voltage: 1.2 V
 - Total PDN Margin % / mV: 3.5% / 42 mV @ 1.2 V
 - Z_{target} (up to 1 MHz): 1 mΩ
 - Z_{target} (1 MHz to 10 MHz): 6 mΩ

The decoupling capacitors are also required to keep the impedance profile of this power rail under Z_{target} .

Note: RDIMM part number M393ABG40M52 has been used for calculation, with $\text{IDD}_{\text{max}} = 23.3$ A. Each power rail +1V2_VDDQx has 8x R-DIMM (186.4 A) + 4x MCU (10 A).

4.1.2 Decoupling Requirements to Achieve Target Impedance

To achieve the target impedance in a wide range of frequency, the designer must choose to vary decoupling capacitors with the value from low to high. Each capacitor has its own effects within its frequency. Typically, high-value capacitors reduce impedance profile at low frequency whereas capacitors with low-value affect board impedance at high frequency.

From the data in section [4.1.1.2 \(PCP Voltage\)](#), [Table 8](#) lists examples of the decoupling capacitors for the +0V75_PCP_S0 power rail. Note that the decoupling capacitors need to run a PI simulation for verification and optimization.

Table 8: +0V75_PCP_S0 Decoupling Capacitors

GROUP #	VALUE (μF)	NO. OF CAPS	DESCRIPTION	MANUFACTURER	PART #	ESR (mΩ)
1	1	6	CAP CER 1 μF 25 V X6S 0402	Taiyo Yuden	TMK105AC6105KV-F	6.2
2	2.2	31	CAP CER 2.2 μF 4 V X5R 0402	Taiyo Yuden	JMK105BJ225MV-F	6.1
3	4.7	33	CAP CER 4.7 μF 10 V X5R 0402	Samsung	CL05A475MP5NRNC	6.8
4	10	32	CAP CER 10 μF 6.3 V 20% X5R 0402	Murata	GRM155R60J106ME15D	6
5	22	63	CAP CER 22 μF 6.3 V 20% X5R 0603	TDK	C1608X5R0J226M080AC	3.9
6	220	26	CAP CER 220 μF 4 V X6S 1206	Murata	GRM31CC80G227ME11L	2
7	560	20	SP-CAP, 560 μF, 20%, 2 V, 7343, SMD, 3 mΩ, 10.2 A @ 100 kHz	Panasonic	EEF-GX0D561L	3



From the data in section 4.1.1.3 (SoC Voltage), Table 9 lists examples of the decoupling capacitors for the +0V75_VDDC_SOC_S0 power rail. Note that the decoupling capacitors need to run a PI simulation for verification and optimization.

Table 9: +0V75_VDDC_SOC_S0 Decoupling Capacitors

GROUP #	VALUE (μF)	NO. OF CAPS	DESCRIPTION	MANUFACTURER	PART #	ESR (mΩ)
1	1	6	CAP CER 1 μF 25 V X6S 0402	Taiyo Yuden	TMK105AC6105KV-F	6.2
2	2.2	6	CAP CER 2.2 μF 6.3 V 20% X5R 0402	Taiyo Yuden	JMK105BJ225MV-F	6.1
3	4.7	6	CAP CER 4.7 μF 10 V 20% X5R 0402	Samsung	CL05A475MP5NRNC	6.8
4	10	6	CAP CER 10 μF 6.3 V 20% X5R 0402	Murata	GRM155R60J106ME15D	6
5	22	9	CAP CER 22 μF 6.3 V 20% X5R 0603	TDK	C1608X5R0J226M080AC	3.9
6	220	5	CAP CER 220 μF 4 V X6S 1206	Murata	GRM31CC80G227ME11L	2
7	560	5	SP-CAP, 560 μF, 20%, 2 V, 7343, SMD, 3 mΩ, 10.2 A @ 100 kHz	Panasonic	EEF-GX0D561L	3

Table 10 lists examples of the decoupling capacitors for the +0V85_VDDC_RCA_S0 power rail. Note that the decoupling capacitors need to run a PI simulation for verification and optimization.

Table 10: +0V85_RCA_S0 Decoupling Capacitors

GROUP #	VALUE (μF)	NO. OF CAPS	DESCRIPTION	MANUFACTURER	PART #	ESR (mΩ)
1	0.01	4	CAP, .01 μF, X7R, 25 V, 10%, 0402	Yageo	CC0402KRX7R8BB103	22
2	0.1	4	CAP 0.1 μF X7R 16 V 10% 0402	Murata	GRM155R71C104KA88D	20
3	4.7	8	CAP CER 4.7 μF 10 V 20% X5R 0402	Samsung	CL05A475MP5NRNC	6.8
4	10	18	CAP CER 10 μF 6.3 V 20% X5R 0402	Murata	GRM155R60J106ME15D	6
5	22	3	CAP CER 22 μF 6.3 V 20% X5R 0603	TDK	C1608X5R0J226M080AC	3.9
6	220	5	CAP CER 220 μF 4 V X6S 1206	Murata	GRM31CC80G227ME11L	2
7	560	5	SP-CAP, 560 μF, 20%, 2 V, 7343, SMD, 3 mΩ, 10.2 A @ 100 kHz	Panasonic	EEF-GX0D561L	3



From the data in section [4.1.1.5 \(DDR Voltage\)](#), [Table 11](#) lists examples of the decoupling capacitors for the +1V2_VDDQ0123_S0 power rail. The same table is applicable for +1V2_VDDQ04567_S0.

Note that the decoupling capacitors need to run a PI simulation for verification and optimization.

Table 11: +1V2_DDQ0123_S0 Decoupling Capacitor

GROUP #	VALUE (μF)	NO. OF CAPS	DESCRIPTION	MANUFACTURER	PART #	ESR (mΩ)
1	4.7	36	CAP CER 4.7 μF 10 V X5R 0402	Samsung	CL05A475MP5NRNC	6.8
2	10	4	CAP CER 10 μF 6.3 V 20% X5R 0402	Murata	GRM155R60J106ME15D	6
3	22	83	CAP CER 22 μF 6.3 V 20% X5R 0603	TDK	C1608X5R0J226M080AC	3.9
4	220	10	CAP CER 220 μF 4 V X6S 1206	Murata	GRM31CC80G227ME11L	2
5	560	10	SP-CAP, 560 μF, 20%, 2 V, 7343, SMD, 3 mΩ, 10.2 A @ 100 kHz	Panasonic	EEF-GX0D561L	3

4.1.3 Voltage Regulator Power Efficiency

- TDP: 250 W
- PMD Current (I_{PCP}): 240 A

For detailed information on the operating frequencies, Thermal Design Power (TDP), and related power numbers, refer to the section titled *Power Specifications* in the Altra Datasheet.

4.1.4 Min/Max Voltages for I/O Power Rails

For detailed information on key voltage rails, refer to the section titled *Recommended Operating Conditions* in the Altra Datasheet.

4.1.5 I/O Voltage Filter Requirements

- Altra requires I/O voltage filters for the following input pins:
 - VDDC_RCA0/1/2/3
 - VDDC_RCB0/1/2/3
 - VDDH_RCA0/1/2/3
 - VDDH_RCB0/1/2/3
 - VDDC_SOC_CLKBUFF_AVDD
 - VDD18_SERDES_AVDD
 - VDD18_DDR_AVDD
 - VDD18_PCP_AVDD
- Filter requirements (cut off frequency) and example schematics: Refer to the section titled [Power Supply Filtering and Decoupling](#) for more information.

4.1.6 Power Supply Management

4.1.6.1 PMBus Based Register Access

- Required to use AVS feature
- Optional for non-AVS applications

4.1.6.2 Telemetry (PMBus Access Required)

- Vout Control



- Voltage and Current (Power) monitor
- Temperature monitor

4.1.6.3 VR Protection and Alarm Signals

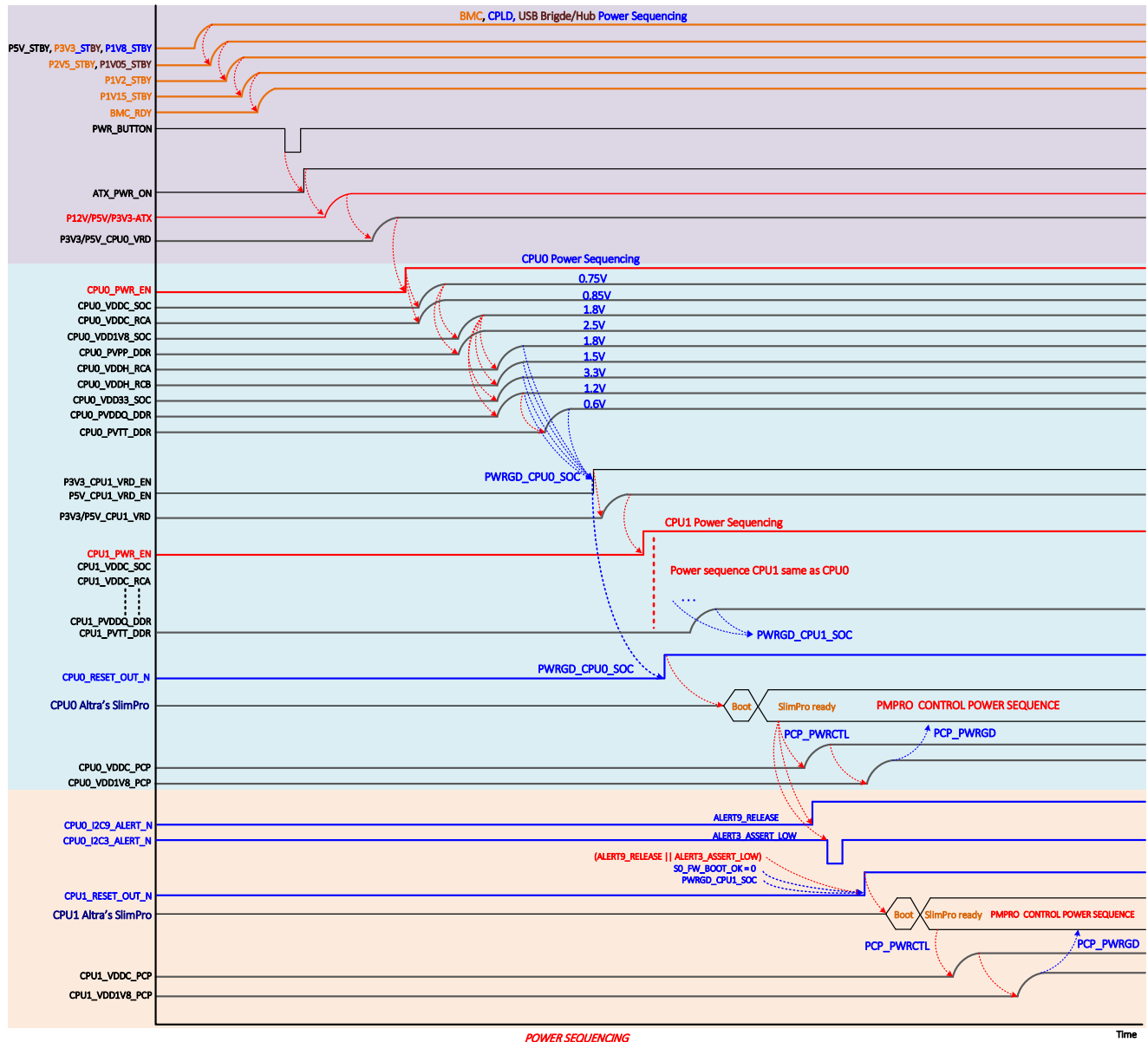
- Over/under voltage protection
- Overcurrent protection
- Overtemperature protection



4.1.7 Power Sequencing

This section outlines the power sequencing requirements for the Altra SoC. Altra is connected to an external power control device that is used to drive the power supplies and inform Altra when the power supplies for the SoC and PCP power domains are stable. [Figure 37](#) shows the flowchart which outlines the power sequencing steps followed by Altra when powering up. Additional details related to the power sequencing can be found in the section titled *Power Supply Sequencing* in the Altra Datasheet.

Figure 37: Altra Power Supply Sequencing



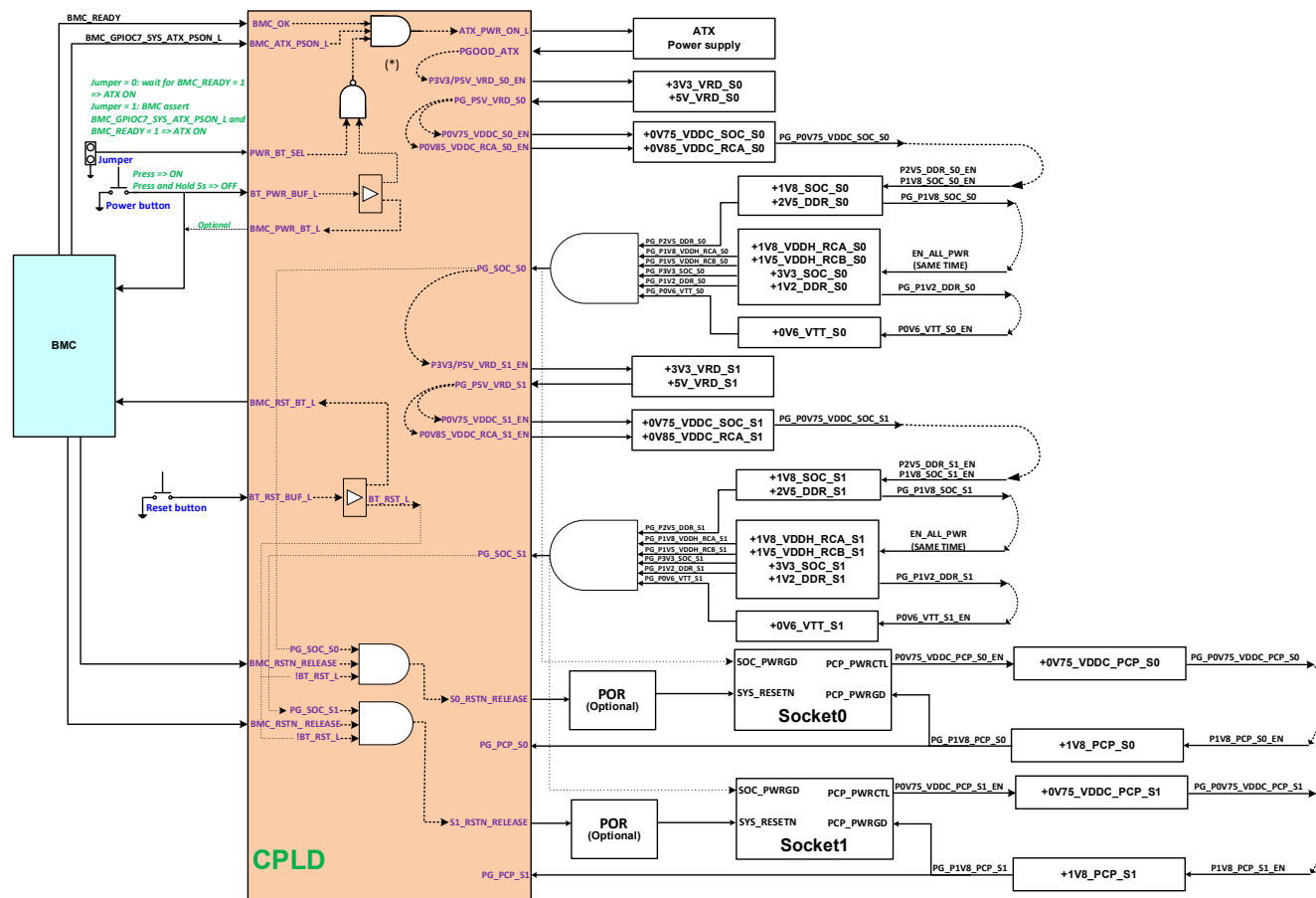
The external control circuit (such as CPLD or BMC) controls the first VRD of Socket0 (S0 or CPU0) in the sequencing – VDDC_SOC (+0V75_VDDC_SOC_S0) and SerDes Core (+0V85_VDDC_RCA_S0). The PowerGood of VDDC_SOC VRD is used to enable +1V8_SOC_S0 regulator which provides power for VDD18_SOC pins.

Next, +1V8_SOC_S0 regulator's PowerGood is used to enable remaining regulators in SOC domain, including +1V8_VDDH_RCA_S0, +1V5_VDDH_RCB_S0, +3V3_SOC_S0, +1V2_VDDQ*_S0 and an external power supply +2V5_DDR*_S0 for DIMM. There is no particular sequencing required among these regulators. CPU SOC domain power sequence in addition

to ramping up power supplies requires providing two system signals: SOC PowerGood to SOC_PWRGD pin of Altra and system reset (controlled by CPLD) CPLD_Socket0_RST#.

Figure 38 shows the CPLD controlled power-up sequence.

Figure 38: CPLD Controlled Power Up Sequence



Once Socket0 (CPU0) SOC domain powers up successfully, the external CPLD or BMC continues to toggle enable signals of Socket1 (CPU1) VRD. The power sequence of CPU1's SOC domain is the same as the sequence of CPU0's SOC domain.

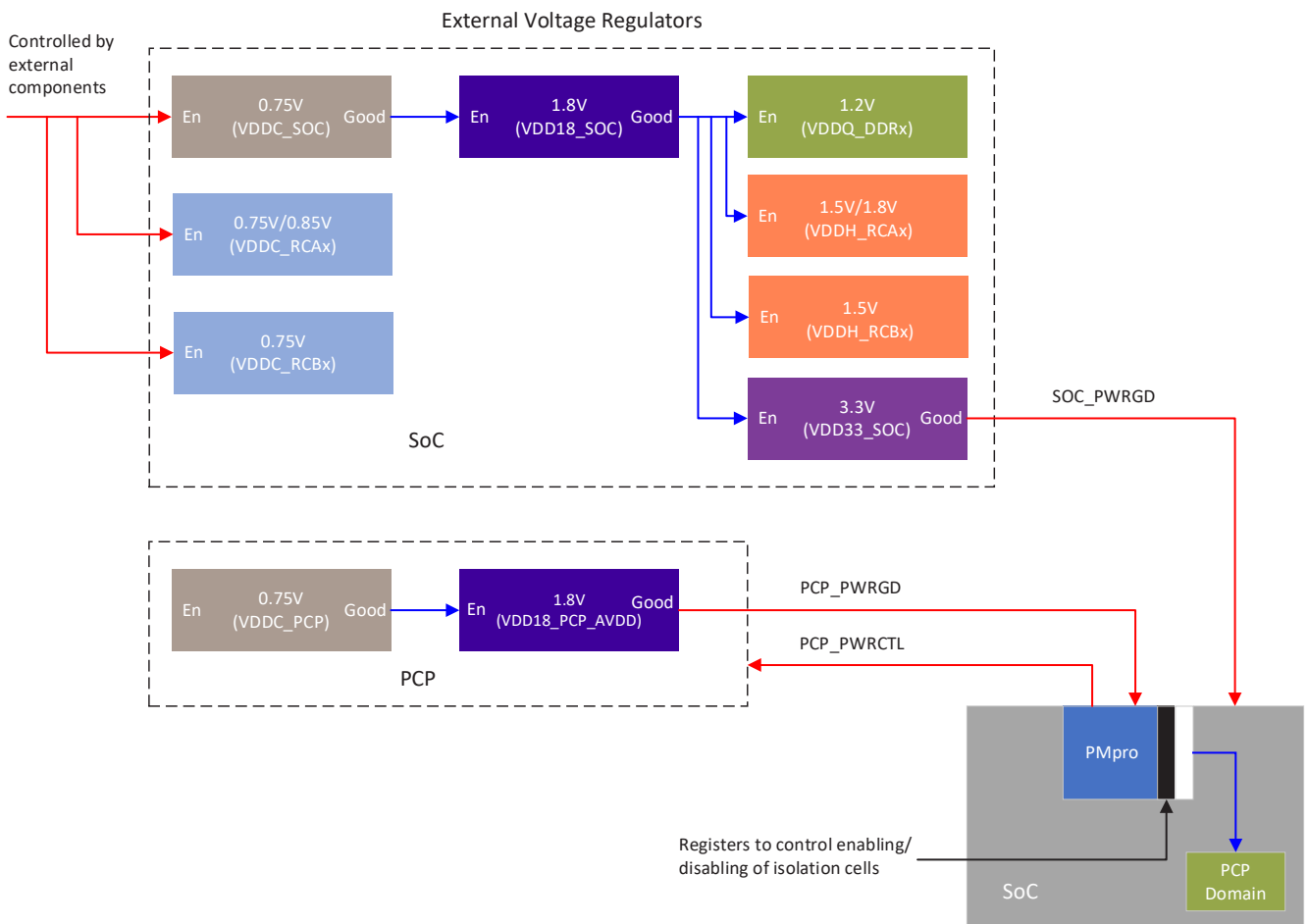
After both CPU0 and CPU1's SOC domains power up successfully, the CPLD releases both Socket0_RST# and Socket1_RST# at the same time.

The CPU0 PCP domain power sequence is controlled by PMPro and is enabled by PCP_PWRCTL pin. After the CPU0 is out of reset, CPU0 accesses the EEPROM and boots up first and pulls the ALERT9_N pin low. CPU0 PMPro enables +0V75_PCP_S0 VRD and then, PowerGood of +0V75_PCP_S0 enables +1V8_PCP_S0 power rails. The PowerGood of VDD18_PCP (+1V8_PCP_S0) is input to CPU0's PCP_PWRGD pin. Power sequencing of Socket0 is completed when this CPU0's PCP_PWRGD goes high, and Socket0 releases ALERT9_N for this signal to go high.

CPU1 detects the ALERT9_N as high and is ready to access the EEPROM and to boot-up. CPU1 PMPro enables +0V75_PCP_S1 VRD and then, PowerGood of +0V75_PCP_S1 enables the +1V8_PCP_S1 power rail. The PowerGood of VDD18_PCP (+1V8_PCP_S1) is input to CPU1's PCP_PWRGD pin. Power sequencing of Socket1 will be completed when this CPU1's PCP_PWRGD goes high.



Figure 39: System Configuration using Two Voltage Regulators



4.1.8 Dynamic Voltage and Frequency Scaling (DVFS)

Altra's maximum frequency mode is implemented based on DVFS, which requires fast access to voltage regulators through PMBus, higher than 400 kHz. Since the maximum frequency mode is implemented on PCP power rail only, the higher speed PMBus access is required for the voltage regulator on PCP power rail. Altra uses I2C interface to implement PMBus protocol over VR.



- Dynamic output voltage transitions with programmable slew rates via PMBus interface
- PMBus supports speeds of 100 kHz, 400 kHz and 1 MHz
- Voltage regulator supplies for VDDQ_DDR* and VPP_DDR* (e.g. Texas Instruments TPS53679)
 - One dual-channel (5-Phase +1-Phase) D-CAP+™ step-down multiphase controller for each 4-DDR4-channel, one 5-Phase supports up to 8 DIMMs (195 A max) and the remaining phase (15A max) supplies DIMMs' VPP power. This design requires totally 4 VRDs for all 32 DIMMs.
 - Full VR13 server feature set including digital input power monitor and PIN_ALT pin
 - PMBus™ system interface for telemetry of voltage, current, power, temperature, and fault conditions
 - Dynamic output voltage transitions with programmable slew rates via PMBus interface
 - PMBus supports speed 100 kHz, 400 kHz and 1 MHz
- VTT_DDR* voltage regulator (e.g. Texas Instruments TPS53317)
 - Supports DDR memory termination with up to 6 A continuous output source or sink current to 8 DIMMs per VRD. The whole design requires totally 4 VRDs for all 32 DIMMs.
- PLL/I/O/SerDes Voltage Regulator (e.g. Texas Instruments TPS53915)
 - The CPU PLL/I/O/SerDes power rails require a variety of voltages including VDD18_SOC, VDD33_SOC and VDDH_RCA/B[0:3].
 - By using the TI TPS53915 (12 A Step-Down Regulator With Integrated Switcher), they can provide precise voltages to these power rails.
 - VDD18_PCP has the same voltage as VDD18_SOC, therefore, to save cost, one MOSFET per Altra is used to switch power from VDD18_SOC and supply to these power pins.
- Miscellaneous voltage regulators
 - Besides CPU power, it is necessary to supply other powers to external devices such as clock generators, Ethernet PHY, PCIe card, HDD/M.2 NVMe, VGA, fans and many other devices. These require different voltages (e.g. 12V, 5V, 3V3) with varying current ratings.
 - To ensure that the voltage regulators can handle the maximum current rating and obtain high efficiency, the designer must calculate the power consumption carefully, then, choose proper voltage regulators that meet these requirements.
- BMC voltage regulator
 - The BMC domain also requires many power supplies for its power and devices connected to it. Typically, BMC requires +1.15V to VCORE, +1.2V to I/O, +2.5V to SDRAM, +3.3V to external devices and +5V to USB devices.

4.2.2 Reference Layout

Refer to the document titled *Altra PCB Layout Guidelines* available on Ampere Computing's Customer Connect portal at <https://connect.amperecomputing.com>.



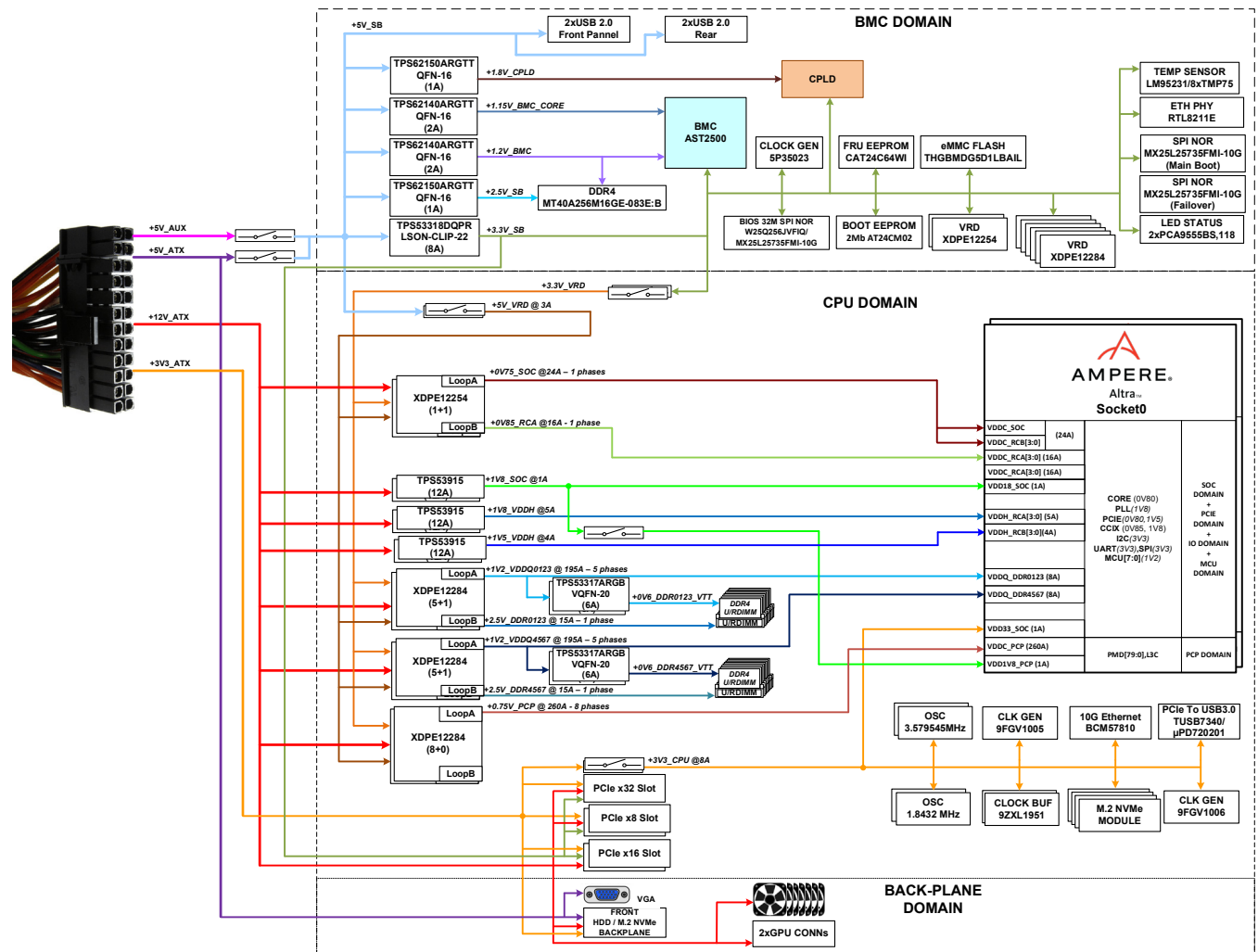
4.3 VRD Implementation using Infineon Devices

4.3.1 Overview of IR Voltage Regulators

Optionally, IR VRD devices can be chosen to design power supplies as illustrated in [Figure 41](#).

- Voltage regulator supplies for VDDC_PCP (e.g. XDPE12284)
 - One channel (8-Phase) multiphase controller per Altra, one 8-phase rail for VDDC_PCP supporting up to 300 A.
 - Full VR13 server feature set including digital input power monitor and PIN_ALT pin
 - PMBus™ system interface rev 1.2 compliant for telemetry of voltage, current, power, temperature, and fault conditions
 - Dynamic output voltage transitions with programmable slew rates via PMBus interface
 - PMBus supports speeds of 100 kHz, 400 kHz.

Figure 41: VRD Power Diagram for Dual-Socket Platforms using Infineon Devices



- Voltage regulator supplies for VDDC_SOC and VDDC_RCA (e.g. XDPE12254)
 - One dual-channel (1-Phase + 1-Phase) multiphase controller per Altra, one 1-phase rail for VDDC_SOC supporting up to 26.67 A and the remaining 1-phase for VDDC_RCA supporting 16A.
 - Full VR13 server feature set including digital input power monitor and PIN_ALT pin
 - PMBus™ system interface rev 1.2 compliant for telemetry of voltage, current, power, temperature, and fault conditions
 - Dynamic output voltage transitions with programmable slew rates via PMBus interface



- PMBus supports speeds of 100 kHz, 400 kHz.
- Voltage regulator supplies for VDDQ_DDR* and VPP_DDR* (e.g. XDPE12284)
 - One dual-channel (5-Phase + 1-Phase) multiphase controller for each 4-DDR4-channel, one 5-Phase supports up to 8 DIMMs (195 A max) and the remaining phase (30 A max) supplies DIMMs' VPP power. This design requires totally 4 VRDs for all 32 DIMMs.

4.3.2 Reference Layout

Refer to the document titled *Altra PCB Layout Guidelines* available on Ampere Computing's Customer Connect portal at <https://connect.amperecomputing.com>.

4.4 Power Integrity Simulations

The designer must run the PI simulation including Analyze DC drop and AC decoupling of main power rails which consume high currents, such as +0V75_VDDC_PCP, +0V75_VDDC_SOC, +1V2_DDR0123, and +1V2_DDR4567. The following items must be considered:

- DC Drop analysis:
 - This exposes area of power planes that are narrow or places where voltage drop is excessive.
 - This can help determine needs for high current trace widths, stitching via quantities and overall design insight.
 - Determine the max DC resistance for every power rail.
- AC Decoupling analysis:
 - This considers the maximum budget voltage with the constraints of maximum power supply ripple, target impedance, peak transient current of Altra.
 - Show the PDN (Power Distribution Network) in the frequency domain.
 - The goal is to determine the number of capacitor values enough to bring the impedance profile below the target impedance.

Cadence Sigrity v17.2 or Mentor Graphics Hyperlynx v9.4 PI simulation tools can be used to perform this task.



4.4.1 Simulation Results

4.4.1.1 VDDC_PCP

1. DC Drop analysis
 - a) Simulation setup:
 - Reference Voltage for Margin: 1.0 V
 - Maximum DC-Resistance Specification for both Altra QS80-30 and Altra QS80-33: 0.2 mΩ
 - Maximum Current:
 - Total Max Current: 300 A (QS80-33) or 267 A (QS80-30), in 3 steps (see [Figure 42](#) below)
 - Max Current Instantaneous Step: 225 A (QS80-330) or 204 A (QS80-30) (Step 3)
 - Follow step function for VDDC_PCP for simulations as shown in [Figure 42](#).
 - **Note:** Voltage for QS80-33 is raised to 1.08 V to maintain margin.

Figure 42: Voltage Drop Example (Idealized, Not to Scale)

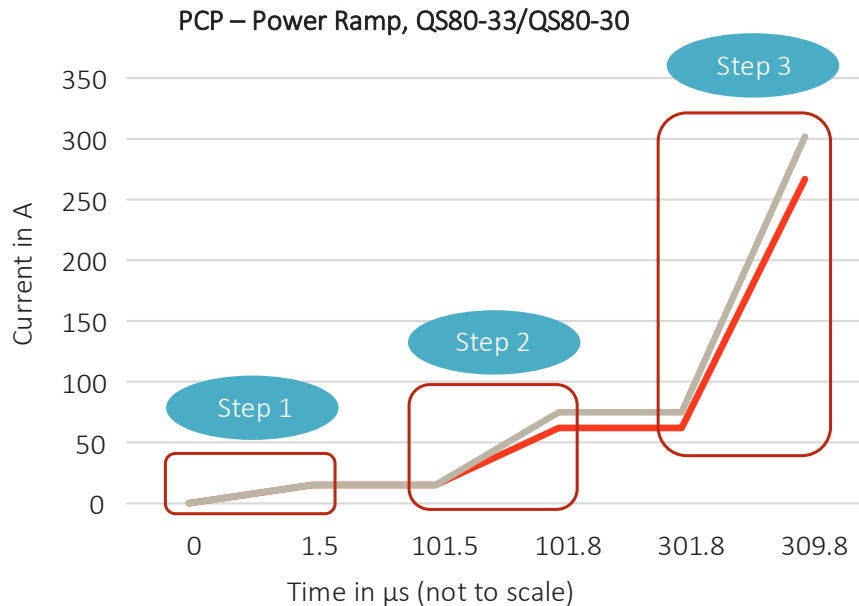


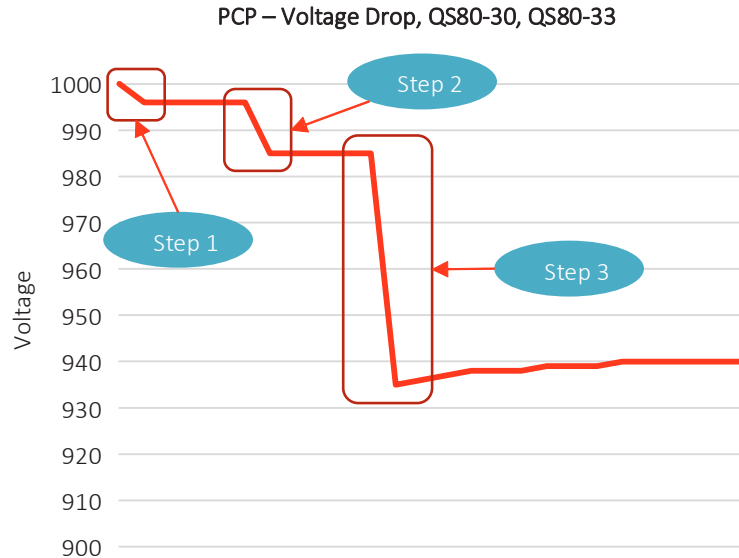
Table 12: PCP Power Ramp Steps

MAX CURRENT STEPS	Altra QS80-30	Altra QS80-33
Max Current Step 1	0 to 15 A in 1.5 μs at 1.0 V	0 to 15 A in 1.5 μs at 1.08 V
Max Current Step 2	15 A to 62 A in 0.3 μs at 1.0 V	15 A to 75 A in 0.3 μs at 1.08 V
Max Current Step 3	62 A to 267 A in 8 μs at 1.0 V	75 A to 300 A in 8 μs at 1.08 V



b) Simulation results: Refer [Figure 43](#)

Figure 43: Voltage Drop Example (Idealized, Not to Scale)



2. AC Decoupling analysis

a) Simulation setup for QS80-30:

- Peak Transient Current: 204 A in 8 μ s at 1.0 V
- Maximum percentage AC drop (including VRM DC-error and Ripple): 5%

b) Simulation setup for QS80-33:

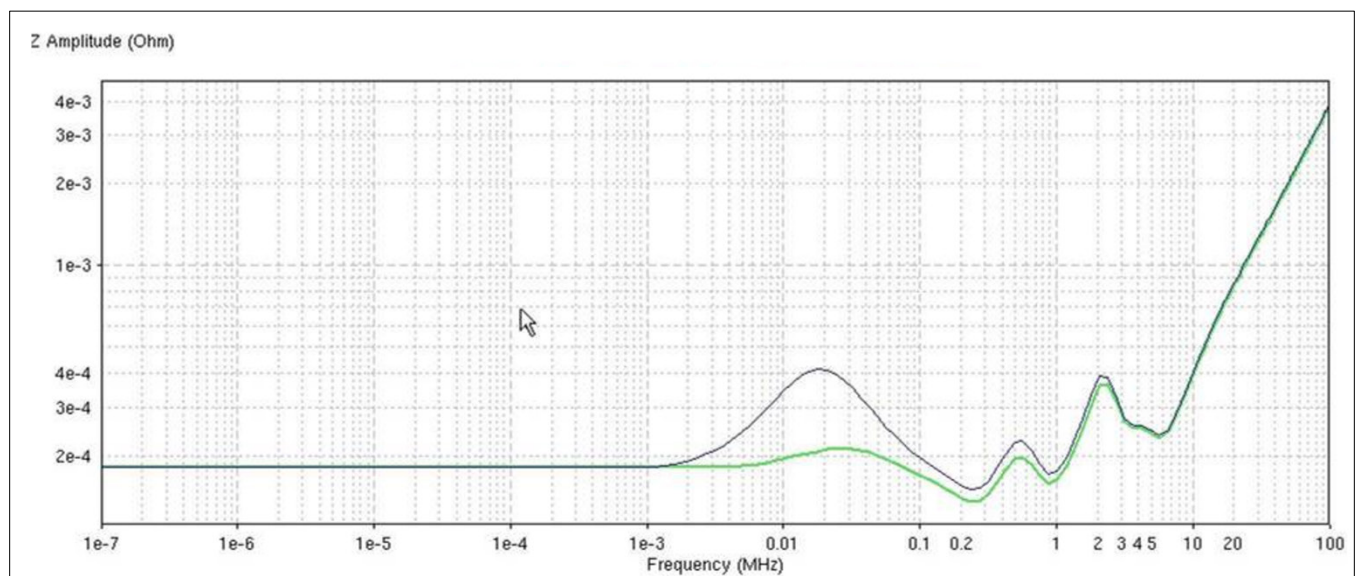
- Peak Transient Current: 225 A in 8 μ s at 1.0 V
- Maximum percentage AC drop (including VRM DC-error and Ripple): 8%

c) Target Impedance for both Altra QS80-30 and Altra QS80-33:

- Z_{target} , up to 1 MHz: 0.3 m Ω
- Z_{target} , 1 MHz to 10 MHz: 0.4 m Ω

d) Simulation-based Frequency Domain results: Refer [Figure 44](#)

Figure 44: VDDC_PCP PCB-Only Frequency Domain Impedance Plot





Note:

- Green is the Z-plot without VRM inductors.
- This is a PCB-only plot based on Altra Mt. Jade Reference Design, and is subject to change.

4.4.1.2 VDDC_SOC

- DC Drop analysis
 - Simulation setup:
 - Reference Voltage for Margin: 0.75 V
 - Maximum DC-Resistance Specification for both Altra QS80-30 and Altra QS80-33: 1.1 mΩ
 - Maximum current:
 - Total Max Current: 26.67 A, in 3 steps (see [Figure 45](#) below)
 - Follow step function for VDDC_SOC for simulations as shown in [Figure 45](#).

Figure 45: VDDC_SOC Max Current Ramp Rate and Current Step

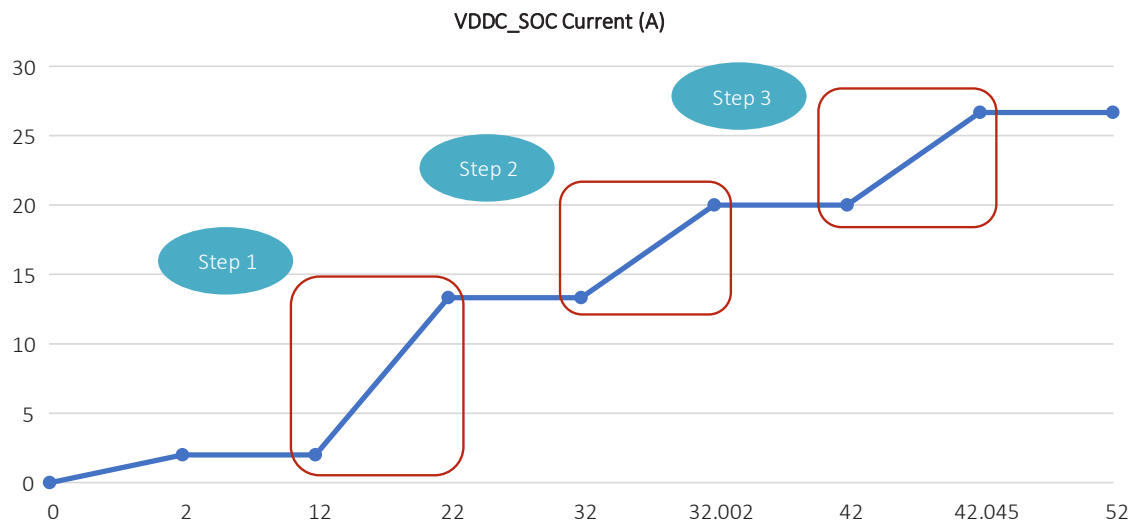


Table 13: VDDC_SOC Max Current Ramp Rate and Current Step

MAX CURRENT STEPS	Altra QS80-30	Altra QS80-33
Max Current Step 1, at 0.75 V	2 A to 13.33 A in 10 μs	
Max Current Step 2, at 0.75 V	13.33 A to 20 A in 2 ns	
Max Current Step 3, at 0.75 V	20 A to 26.67 A in 4.5 ns	



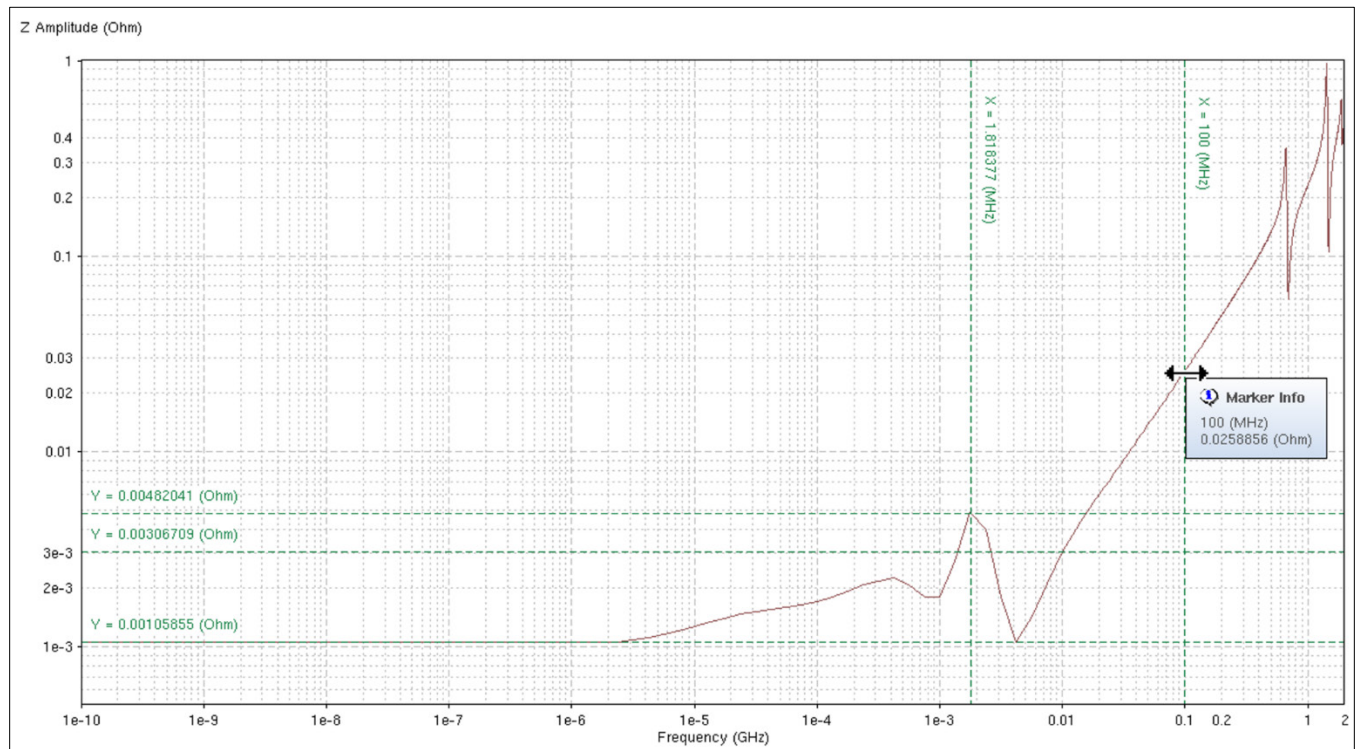
2. AC Decoupling analysis

a) Simulation setup:

- Peak Transient Current: 13.33 A (two-step) at 6.5 ns
- Maximum percentage AC drop (including VRM DC-error and Ripple): 5%
- Target Impedance for both Altra QS80-30 and Altra QS80-33:
 - Z_{target} , up to 1 MHz: 2 mΩ
 - Z_{target} , 1 MHz to 10 MHz: 5 mΩ

b) Simulation results: Refer [Figure 46](#)

Figure 46: VDDC_SOC PCB-Only Frequency Domain Impedance Plot



Note:

- Z-plot without VRM inductors
- VDD_SOC S-param port assigned at SOC-package balls
- This is a PCB-only plot based on Altra Mt. Jade Reference Design, and is subject to change.



4.4.1.3 VDDC_RCA

1. DC Drop analysis
 - a) Simulation setup:
 - Voltage: 0.85 V
 - Maximum Current: 16 A
 - Maximum DC-Resistance Specification for both Altra QS80-30 and Altra QS80-33: 20 mΩ

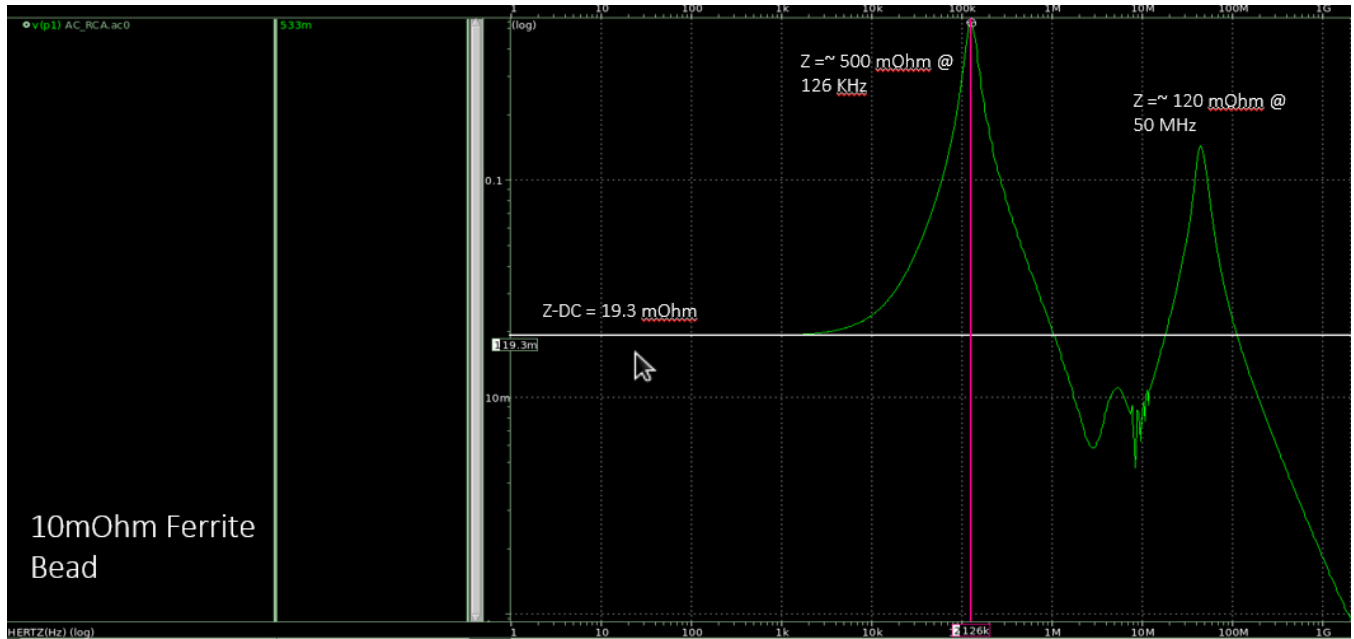
Table 14: VDDC_RCA Mission-mode Steady-state Current Calculation Based on PHY Data Book Specifications

MODE		CURRENT FROM vp (mA)	CURRENT FROM vptx (mA)	CURRENT FROM vph (mA)	CURRENT FROM vpdig (mA)	TOTAL CURRENT (mA)
PO	25 Gbps Typ	170.100	259.200	260.700	43.070	733.070
	25 Gbps Wc	254.100	362.600	303.300	120.400	1040.400
• WC current per x4 PHY = 0.74 A – Typ current per x4 PHY = 0.47 A • WC current for four x4 PHYs = 0.74 x 4 = 2.96 A • Controller logic current calculation @ 0.85 V = 1.74 A • Total RCA current (worst-case) = 4.7 A						

2. AC Decoupling analysis
 - a) Simulation setup:
 - Peak Transient Current above and below steady-state current draw during mission-mode: 260 mA at 50 MHz to maximize excitation of the anti-resonance peak at around 50 MHz
 - Maximum percentage AC drop (including VRM DC-error and Ripple): 5%
 - Z_{target} , up to 1 MHz: 500 mΩ
 - Z_{target} , 1 MHz to 50 MHz: 120 mΩ
 - b) Simulation results:
 - The impedance profiles of +0V85_VDDC_RCA on the Altra Validation board are below the target impedance specifications.



Figure 47: VDD_RCA PCB-Only Frequency Domain Impedance Plot – with 10 mΩ Ferrite Bead



4.4.1.4 +1V2_VDDQ0123/4567

1. DC Drop analysis at CPU
 - a) Simulation setup:
 - Reference Voltage for Margin: 1.2 V
 - Maximum DC-Resistance Specification for both Altra QS80-30 and Altra QS80-33: 1 mΩ
 - Maximum current:
 - Total Max Current: 10 A (per half)
 - Follow step function for VDDQ_0123/4567 for simulations as shown in [Figure 48](#).

Figure 48: VDDQ_0123/VDDQ_4567 Max Current Ramp Rate and Current Step

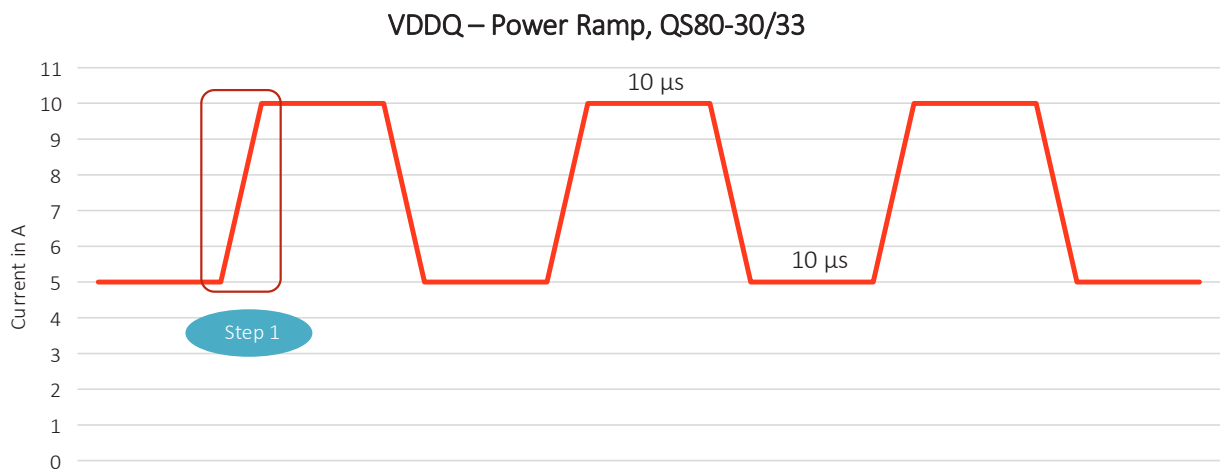


Table 15: VDDQ_0123/4567 Max Current Ramp Rate and Current Step

MAX CURRENT STEPS	Altra QS80-30	Altra QS80-33
Max Current Step 1, at 1.2 V	5 A to 10 A in 2 ns	

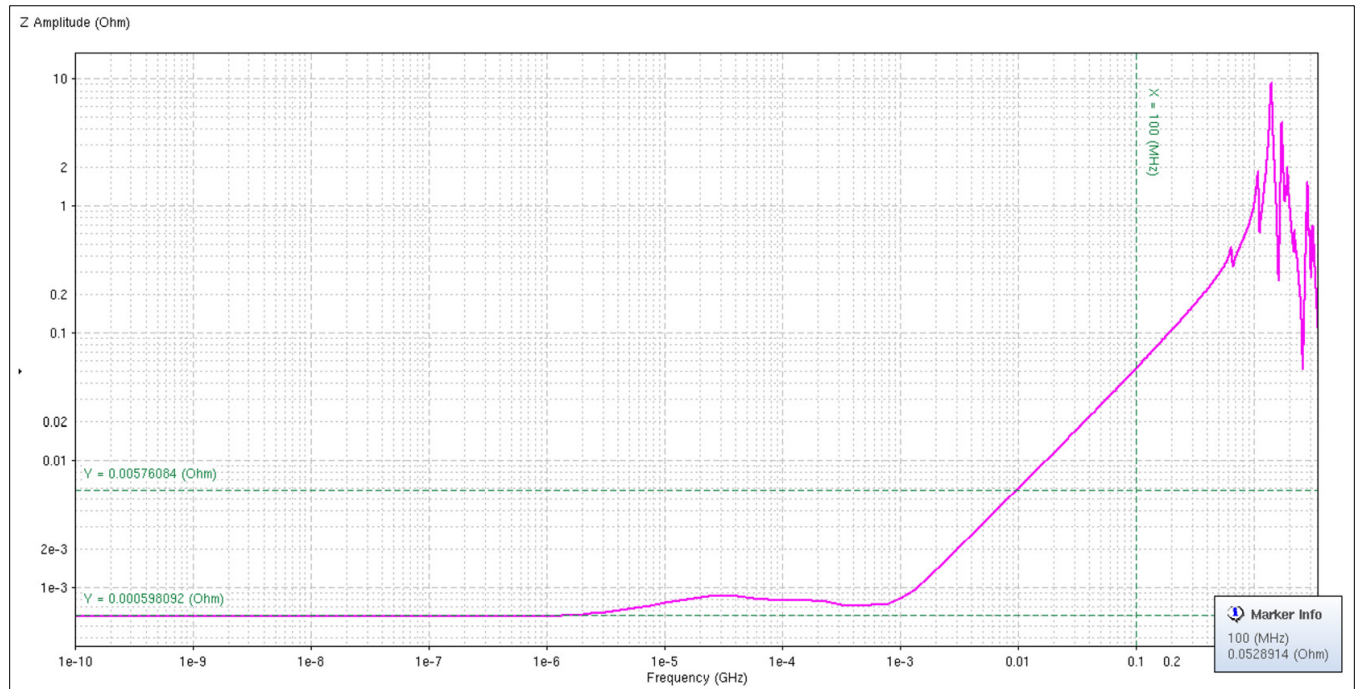


2. AC Decoupling analysis at CPU

a) Simulation setup:

- Peak Transient Current: 5 A in 2ns at 1.2 V
- Maximum percentage AC drop (including VRM DC-error and Ripple): 3.5%
- Target Impedance for both Altra QS80-30 and Altra QS80-33:
 - Z_{target} , up to 1 MHz: 1 m Ω
 - Z_{target} , 1 MHz to 10 MHz: 6 m Ω

Figure 49: VDDQ_0123 PCB-Only Frequency Domain Impedance Plot



Note:

- Z-plot without VRM inductors
- VDDQ0123 S-param port assigned at SOC-package balls
- This is a PCB-only plot based on Altra Mt. Jade Reference Design, and is subject to change.

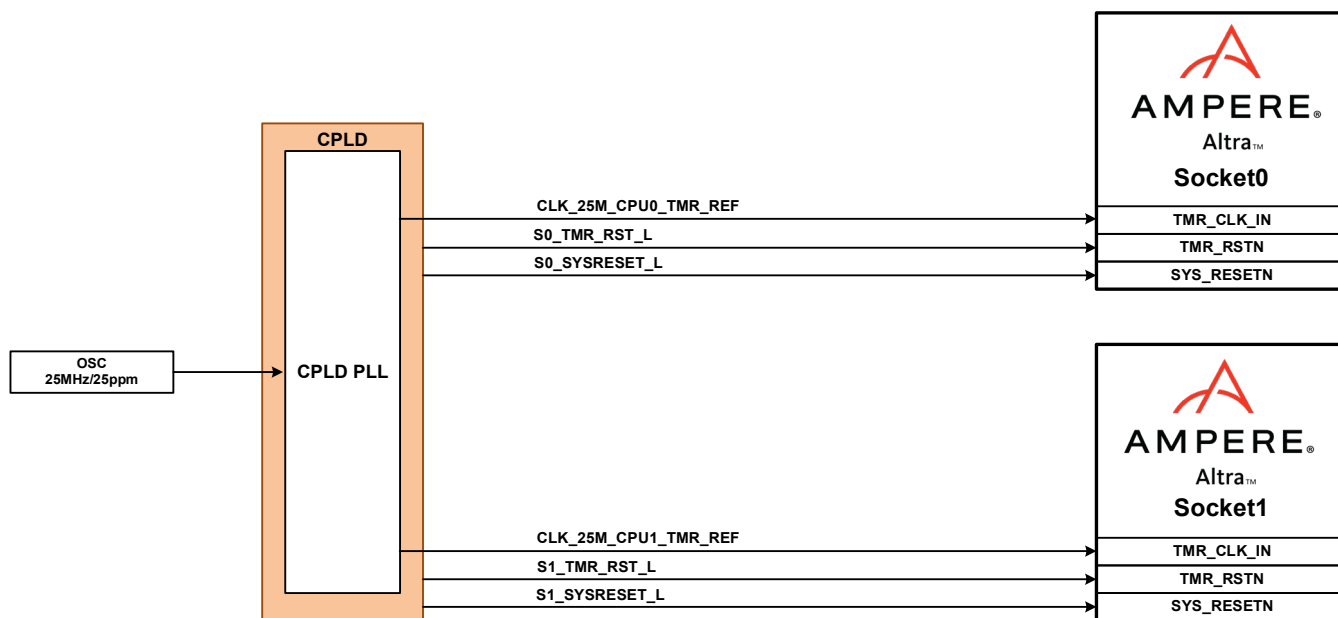


5.1.3 Schematic Guides

- Altra requires two input differential clocks, both of which are PCI Express Gen4 compliant. SYS_REFCLK1 is not spread-spectrum, while SYS_REFCLK2 is spread-spectrum. Internally, any SerDes can be connected to either of the clock inputs, giving the system designer the flexibility of supporting a mix of spread-spectrum and nonspread-spectrum ports.
- The source clocks for Altra reference clocks must be CML 100 MHz.
- Other reference clocks for PCIe Add-in Card and BMC must also be HCSL 100 MHz that follow PCIe specifications.

5.2 Miscellaneous Clock Design Guidelines

5.2.1 TMR Clock



TMR_CLK is a 25 MHz clock used to generate the Global Counter that is distributed to both CPUs for their ARCH Timers.

There are three requirements of TMR_CLK_IN and TMR_RSTN as below:

- The PCB trace length of CLK_25M_CPU0_TMR_REF and CLK_25M_CPU1_TMR_REF must be the same
- The PCB trace length of S0_TMR_RST_L and S1_TMR_RST_L must be the same
- TMR_RSTN need to synchronize with SYS_RESETN and TMR_CLK_IN

5.2.2 UART Clock

Altra need to provide clock source 1.8432 MHz for the ARM PL011 UART baud rate generator.

5.2.3 Termination if Unused

In case external reference clock for UART, TMR are not used, they can be left floating.



6. Reset Distribution

Altra has a total of 48 PCIe controllers and does not have a dedicated PEST for each controller.

An alternate solution for PERST per controller: A set of GPIOs (at most 6 GPIOs defined as outputs) are connected to a CPLD which decodes the PCIe reset request and asserts the proper reset to the endpoint.

Altra resets each PCIe device by sequence, either one device at a time, or all devices at the same time. Once Altra outputs GPIO[16:21] to reset End-Point device, it is required to keep output states for a minimum for 10 μ s so that CPLD can capture correct states.

Refer to [Table 16](#) for details of the signals.

6.1 Altra PERST Encode Table

Table 16: Altra PERST Encode

DECIMAL	PERST	SYS_RESET_L	GPIO 21	GPIO 20	GPIO 19	GPIO 18	GPIO 17	GPIO 16	NET NAME	DESCRIPTION	NOTES
	Reset all	0	x	x	x	x	x	x	–	–	This is power on reset or system reset => All PCIe devices must be reset too.
	Release all Resets	1	1	1	1	1	1	1	–	–	After power on or system reset, when software boot complete => Set GPIO[16:21] = 1 for normal operation
62	RCA00 (x4)	1	1	1	1	1	1	0	RCA00_PERST_L	Reset EP of RCA00	– If config PCIe x16, then only RCA00_PERST_L is used – If config 2x PCIe x8, then RCA00_PERST_L and RCA02_PERST_L are used
61	RCA01 (x4)	1	1	1	1	1	0	1	RCA01_PERST_L	Reset EP of RCA01	
60	RCA02 (x4)	1	1	1	1	1	0	0	RCA02_PERST_L	Reset EP of RCA02	
59	RCA03 (x4)	1	1	1	1	0	1	1	RCA03_PERST_L	Reset EP of RCA03	
58	RCA10 (x4)	1	1	1	1	0	1	0	RCA10_PERST_L	Reset EP of RCA10	– If config PCIe x16, then only RCA10_PERST_L is used – If config 2x PCIe x8, then RCA10_PERST_L
57	RCA11 (x4)	1	1	1	1	0	0	1	RCA11_PERST_L	Reset EP of RCA11	



DECIMAL	PERST	SYS_RESET_L	GPIO 21	GPIO 20	GPIO 19	GPIO 18	GPIO 17	GPIO 16	NET NAME	DESCRIPTION	NOTES
56	RCA12 (x4)	1	1	1	1	0	0	0	RCA12_PERST_L	Reset EP of RCA12	and RCA12_PERST_L are used
55	RCA13 (x4)	1	1	1	0	1	1	1	RCA13_PERST_L	Reset EP of RCA13	
54	RCA20 (x4)	1	1	1	0	1	1	0	RCA20_PERST_L	Reset EP of RCA20	– If config PCIe x16, then only RCA20_PERST_L is used – If config 2x PCIe x8, then RCA20_PERST_L and RCA22_PERST_L are used
53	RCA21 (x4)	1	1	1	0	1	0	1	RCA21_PERST_L	Reset EP of RCA21	
52	RCA22 (x4)	1	1	1	0	1	0	0	RCA22_PERST_L	Reset EP of RCA22	
51	RCA23 (x4)	1	1	1	0	0	1	1	RCA23_PERST_L	Reset EP of RCA23	
50	RCA30 (x4)	1	1	1	0	0	1	0	RCA30_PERST_L	Reset EP of RCA30	– If config PCIe x16, then only RCA30_PERST_L is used – If config 2x PCIe x8, then RCA30_PERST_L and RCA32_PERST_L are used
49	RCA31 (x4)	1	1	1	0	0	0	1	RCA31_PERST_L	Reset EP of RCA31	
48	RCA32 (x4)	1	1	1	0	0	0	0	RCA32_PERST_L	Reset EP of RCA32	
47	RCA33 (x4)	1	1	0	1	1	1	1	RCA33_PERST_L	Reset EP of RCA33	
46	RCBOA0 (x2)	1	1	0	1	1	1	0	RCBOA0_PERST_L	Reset EP of RCBOA0	– If config PCIe x8, then only RCBOA0_PERST_L is used – If config 2x PCIe x4, then RCBOA0_PERST_L and RCBOA2_PERST_L are used
45	RCBOA1 (x2)	1	1	0	1	1	0	1	RCBOA1_PERST_L	Reset EP of RCBOA1	
44	RCBOA2 (x2)	1	1	0	1	1	0	0	RCBOA2_PERST_L	Reset EP of RCBOA2	



DECIMAL	PERST	SYS_RESET_L	GPIO 21	GPIO 20	GPIO 19	GPIO 18	GPIO 17	GPIO 16	NET NAME	DESCRIPTION	NOTES
43	RCB0A3 (x2)	1	1	0	1	0	1	1	RCB0A3_PERST_L	Reset EP of RCB0A3	
42	RCB0B0 (x2)	1	1	0	1	0	1	0	RCB0B0_PERST_L	Reset EP of RCB0B0	– If config PCIe x8, then only RCB0B0_PERST_L is used – If config 2x PCIe x4, then RCB0B0_PERST_L and RCB0B2_PERST_L are used
41	RCB0B1 (x2)	1	1	0	1	0	0	1	RCB0B1_PERST_L	Reset EP of RCB0B1	
40	RCB0B2 (x2)	1	1	0	1	0	0	0	RCB0B2_PERST_L	Reset EP of RCB0B2	
39	RCB0B3 (x2)	1	1	0	0	1	1	1	RCB0B3_PERST_L	Reset EP of RCB0B3	
38	RCB1A0 (x2)	1	1	0	0	1	1	0	RCB1A0_PERST_L	Reset EP of RCB1A0	– If config PCIe x8, then only RCB1A0_PERST_L is used – If config 2x PCIe x4, then RCB1A0_PERST_L and RCB1A2_PERST_L are used
37	RCB1A1 (x2)	1	1	0	0	1	0	1	RCB1A1_PERST_L	Reset EP of RCB1A1	
36	RCB1A2 (x2)	1	1	0	0	1	0	0	RCB1A2_PERST_L	Reset EP of RCB1A2	
35	RCB1A3 (x2)	1	1	0	0	0	1	1	RCB1A3_PERST_L	Reset EP of RCB1A3	
34	RCB1B0 (x2)	1	1	0	0	0	1	0	RCB1B0_PERST_L	Reset EP of RCB1B0	– If config PCIe x8, then only RCB1B0_PERST_L is used – If config 2x PCIe x4, then RCB1B0_PERST_L and RCB1B2_PERST_L are used
33	RCB1B1 (x2)	1	1	0	0	0	0	1	RCB1B1_PERST_L	Reset EP of RCB1B1	
32	RCB1B2 (x2)	1	1	0	0	0	0	0	RCB1B2_PERST_L	Reset EP of RCB1B2	
31	RCB1B3 (x2)	1	0	1	1	1	1	1	RCB1B3_PERST_L	Reset EP of RCB1B3	



DECIMAL	PERST	SYS_RESET_L	GPIO 21	GPIO 20	GPIO 19	GPIO 18	GPIO 17	GPIO 16	NET NAME	DESCRIPTION	NOTES
30	RCB2A0 (x2)	1	0	1	1	1	1	0	RCB2A0_PERST_L	Reset EP of RCB2A0	– If config PCIe x8, then only RCB2A0_PERST_L is used – If config 2x PCIe x4, then RCB2A0_PERST_L and RCB2A2_PERST_L are used
29	RCB2A1 (x2)	1	0	1	1	1	0	1	RCB2A1_PERST_L	Reset EP of RCB2A1	
28	RCB2A2 (x2)	1	0	1	1	1	0	0	RCB2A2_PERST_L	Reset EP of RCB2A2	
27	RCB2A3 (x2)	1	0	1	1	0	1	1	RCB2A3_PERST_L	Reset EP of RCB2A3	
26	RCB2B0 (x2)	1	0	1	1	0	1	0	RCB2B0_PERST_L	Reset EP of RCB2B0	– If config PCIe x8, then only RCB2B0_PERST_L is used – If config 2x PCIe x4, then RCB2B0_PERST_L and RCB2B2_PERST_L are used
25	RCB2B1 (x2)	1	0	1	1	0	0	1	RCB2B1_PERST_L	Reset EP of RCB2B1	
24	RCB2B2 (x2)	1	0	1	1	0	0	0	RCB2B2_PERST_L	Reset EP of RCB2B2	
23	RCB2B3 (x2)	1	0	1	0	1	1	1	RCB2B3_PERST_L	Reset EP of RCB2B3	
22	RCB3A0 (x2)	1	0	1	0	1	1	0	RCB3A0_PERST_L	Reset EP of RCB3A0	– If config PCIe x8, then only RCB3A0_PERST_L is used – If config 2x PCIe x4, then RCB3A0_PERST_L and RCB3A2_PERST_L are used
21	RCB3A1 (x2)	1	0	1	0	1	0	1	RCB3A1_PERST_L	Reset EP of RCB3A1	
20	RCB3A2 (x2)	1	0	1	0	1	0	0	RCB3A2_PERST_L	Reset EP of RCB3A2	
19	RCB3A3 (x2)	1	0	1	0	0	1	1	RCB3A3_PERST_L	Reset EP of RCB3A3	
18	RCB3B0 (x2)	1	0	1	0	0	1	0	RCB3B0_PERST_L	Reset EP of RCB3B0	– If config PCIe x8, then only RCB3B0_PERST_L is used



DECIMAL	PERST	SYS_RESET_L	GPIO 21	GPIO 20	GPIO 19	GPIO 18	GPIO 17	GPIO 16	NET NAME	DESCRIPTION	NOTES
17	RCB3B1 (x2)	1	0	1	0	0	0	1	RCB3B1_PERST_L	Reset EP of RCB3B1	– If config 2x PCIe x4, then RCB3B0_PERST_L and RCB3B2_PERST_L are used
16	RCB3B2 (x2)	1	0	1	0	0	0	0	RCB3B2_PERST_L	Reset EP of RCB3B2	
15	RCB3B3 (x2)	1	0	0	1	1	1	1	RCB3B3_PERST_L	Reset EP of RCB3B3	
Note: 0 to 14 are “neutral” states (CPLD does nothing).											

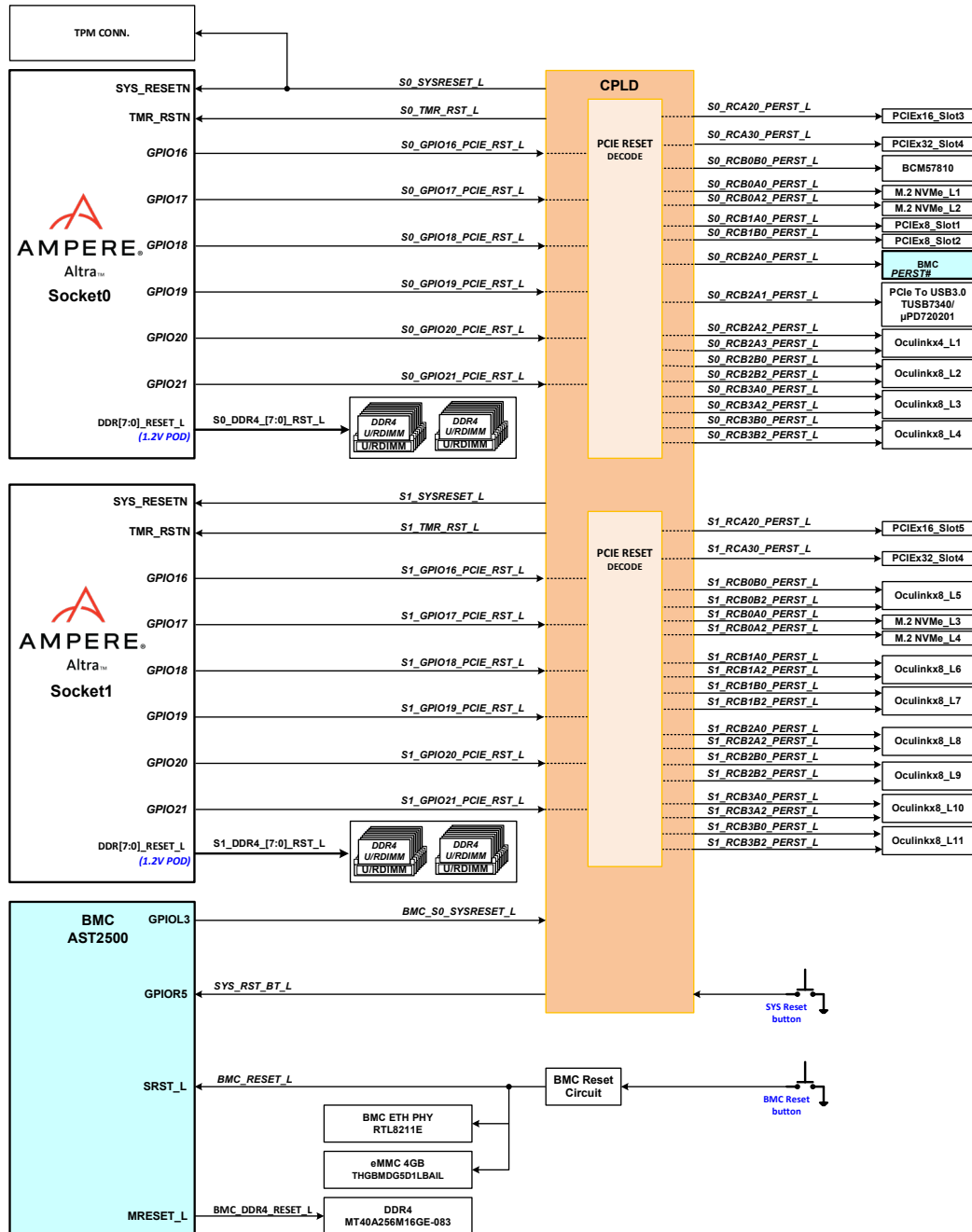


6.2 Design Guidelines

6.2.1 Connectivity

- System Reset button: This is a cold reboot of the mainboard with no effect on BMC's functionality. Upon receiving the System Reset signal from the user, BMC resets the mainboard.
- BMC Reset button: Resets the BMC only, with no effect on the mainboard.

Figure 52: System Reset Diagram



6.2.2 Altra System Reset Requirements

Refer to [Figure 37](#) for details of the Altra power-up sequence. After all power rails are stable, SYS_RESETN must be held LOW for a minimum of 10 μ s.



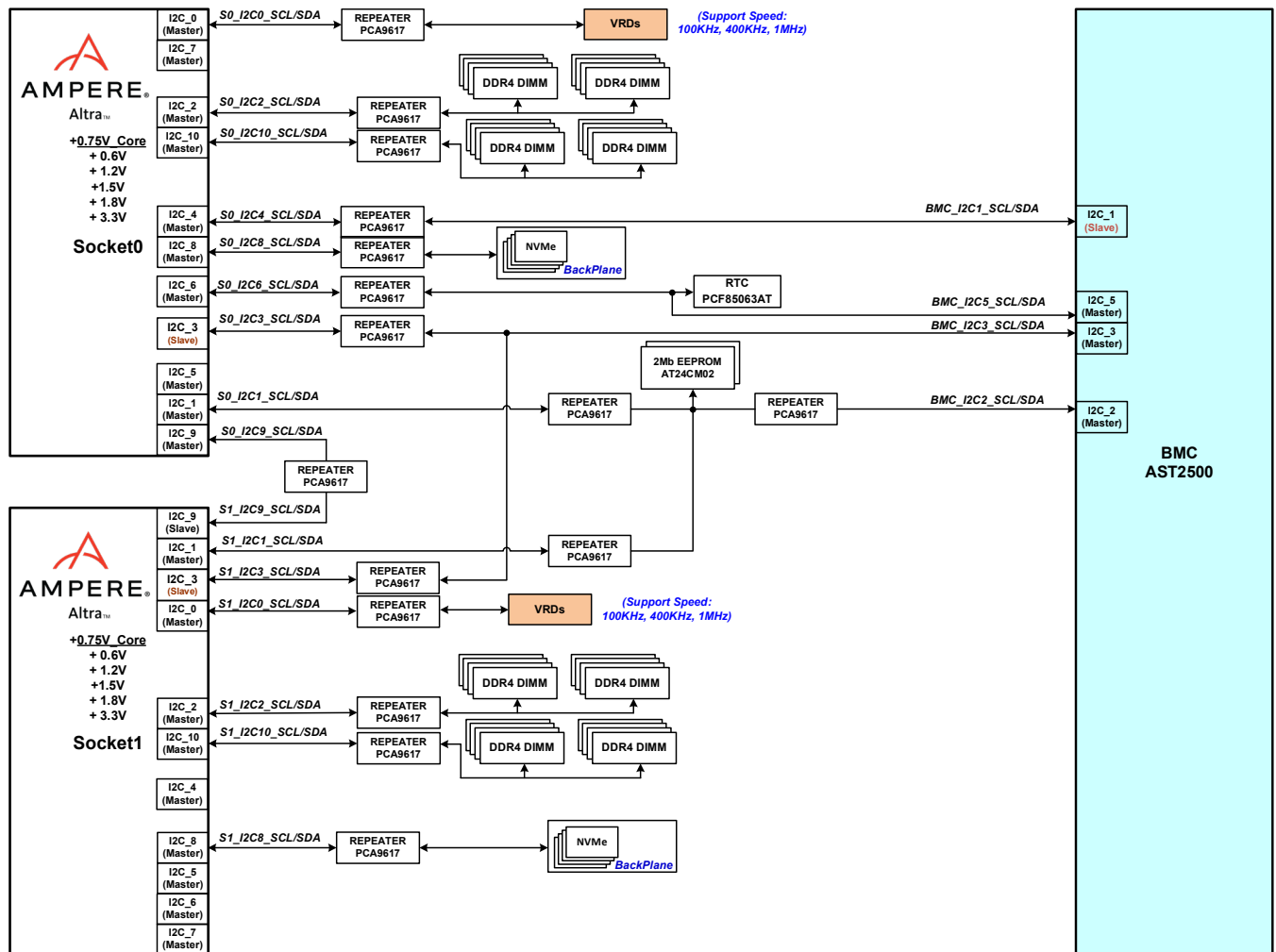
7. Miscellaneous I/O Interfaces

7.1 I2C/SMBus Usage

7.1.1 Design Guidelines

7.1.1.1 Connectivity

Figure 53: I2C Block Diagram for Dual-Socket Platforms





7.1.1.2 Signal Groups

Table 17: I2C Signals

SIGNAL NAME	WIDTH	I/O	I/O TYPE	DESCRIPTION
IIC_SCL_[0:10]	11	I/O	3.3 V LVCMOS 12 mA	I2C Serial Clock. IIC_SCL_[1] is for bootstrap and used in Master mode only. Tri-state output, need external pull-up. Maximum load 150 pF.
IIC_SDA_[0:10]	11	I/O	3.3 V LVCMOS 12 mA	I2C Serial Data. IIC_SDA_[1] is for bootstrap and used in Master mode only. Tri-state output, need external pull-up. Maximum load 150 pF.
PMALERT_N	1	I/O	3.3 V LVCMOS 12 mA	PMBus Alert (active low). Shared alert signal for PMBus. The I2C0 Master port is used as the PMBus Master.
ALERT[1:10]_N	10	I/O	3.3 V LVCMOS 12 mA	Tri-state outputs. Maximum load 150 pF.

7.1.1.3 Schematic Guides

Altra has 11 I2C interfaces with speeds up to 1 MHz. The ports can be a Master or Slave (statically).

- All I2C ports are SMBus 3.0 and PMBus 1.3 capable but without AVSBus support.
- All 9 I2C ports that belong to AHBC block support multi-master.

Each I2C controller can be configured as either a Master or as a Slave. In addition to the I2C clock and data I/O pins, each I2C bus also has an associated SMBus active low ALERT_N I/O pin. When an I2C controller is configured as a Master, the associated ALERT_N I/O pin must be tri-stated and enabled onto one of the internal SPI type interrupts. When configured as a Slave, the ALERT_N I/O pin can be asserted LOW by software to cause an interrupt to the external I2C Master.

[Table 18](#) summarizes the usage of the I2C interfaces available on Altra.

Table 18: Altra I2C Interfaces

I2C DEVICE#	SMB_ALERT	FREQUENCY	MASTER / SLAVE	LOCATION	ACCESSIBILITY	USAGE	I2C OWNER
I2C10	Yes (in) - EVENT# (wired-OR)	1 MHz pt-pt	Master	AHBC	All Optionally S or NS	DDR DIMMs SPD (8 SPDs on west side and configured as NS)	CPUs, SMpro
I2C9	Yes (in for Master and out for Slave)	1 MHz pt-pt	Master for Master socket Slave for Slave socket	AHBC	All Optionally S or NS	Side Communication channel	SMpro



I2C DEVICE#	SMB_ALERT	FREQUENCY	MASTER / SLAVE	LOCATION	ACCESSIBILITY	USAGE	I2C OWNER
I2C8	Yes (in)	1 MHz pt-pt	Master	AHBC	All Optionally S or NS	PCIe Hot-Plug	CPU
I2C7	Yes (in)	1 MHz pt-pt	Master	AHBC	All Optionally S or NS	Board Temp Sensors, Sys EEPROM, and other I2C devices.	SMpro
I2C6	optional	1 MHz pt-pt	Master	AHBC	All Optionally S or NS	RTC	SMpro
I2C5	Yes (in)	1 MHz pt-pt	Master	AHBC	All Optionally S or NS	External TPM and other secure devices (configured as S)	SMpro or CPU
I2C4	Yes (in) - EVENT# (wired-OR)	1 MHz pt-pt	Master	AHBC	All Optionally S or NS	External BMC – SMpro respond to BMC requests	CPU
I2C3	Yes (out) – used to notify BMC of an event on I2C0	1 MHz pt-pt	Slave	AHBC	All Optionally S or NS	External BMC – SMpro receive BMC requests	SMpro
I2C2	Yes (in) - EVENT# (wired-OR)	1 MHz pt-pt	Master	AHBC	All Optionally S or NS	DDR DIMMs SPD (8 SPDs on East side and configured as NS)	CPUs, SMpro
I2C1 + BSC	No	400 kHz	Master	SMpro secure boundary	Private to SMpro	EEPROM for bootstrap vector or SMpro code No other devices must be connected on this bus.	SMpro
I2C0	Yes (in) - VR ALERT output	1 MHz	Master	PMpro	All Secure only	I2C0	Yes (in) - VR ALERT output

- I2C0: Is used to connect to VR SOC/PMD and VR DDR. It is suggested adding I2C translator PCA9617ADP between Altra's I2C0 and VR's I2C when Altra and VR are in different power domains. Also, connect all VRs' I2C/PMBUS alert pin to Altra's I2C0_ALERT# through the isolator.
- I2C1: Is used for boot EEPROM. The boot EEPROM's address must be 0x52. To update EEPROM code through BMC, it is suggested connecting the BMC_I2C to Boot EEPROM via an I2C isolator. Also, add an I2C isolator between Altra's I2C1 and the boot EEPROM.
- I2C2,10: Are used to connect to DDR DIMMs SPD. I2C12 connects to x8 DIMMs SPDs on East side and I2C10 connects to x8 DIMMs SPDs on West. Also, connect all DDR DIMM's Event# to Altra's I2C2/10_ALERT# through the isolator.



- I2C3: Is used as I2C Slave dedicated and connected to BMC's I2C master. The BMC requests Altra through this I2C3 bus. If Altra and BMC are in different power domains, it is suggested adding an I2C Translator PCA9617ADP between Altra's I2C3 and BMC's I2C. Also, connect BMC's I2C_ALERT# to Altra's I2C3_ALERT# through the isolator.
- I2C4: Is used as an I2C master connected to BMC's Slave. BMC responds to Altra's I2C request (I2C read/write). This interface is used as SMBus System interface (SSIF) between the processor and the BMC. If Altra and BMC are in different power domains, it is suggested adding an I2C translator PCA9617ADP between Altra's I2C4 and BMC's I2C. Also, connect BMC's I2C_ALERT# to Altra's I2C4_ALERT# through the isolator.
- I2C5: Is used with external Trusted Platform Module (TPM) and other security devices.
- I2C6: Is used for RTC and shared with BMC's I2C5.
- I2C7: Is used for board Temp Sensor and any other I2C devices
- I2C8: Is used as master connect to NVMe devices on backplane.
- I2C9: Is used to exchange information between two Sockets.

7.1.2 Termination if Unused

When I2C is not used, pull up SCL/SDA, ALERT# to +3V3_SOC_Sx through resistor 4.7 K.

7.1.3 Recommended Device

The flash EEPROM recommended on Altra's I2C1 bus is AT24CM01. This is 1 Mb EEPROM with a 2-page address. It can support speeds up to 1 MHz.

The recommended bus isolator to be used between Altra's I2C and devices/BMC is PCA9617ADP.

7.1.4 Layout Guidelines

SDA/SCL signals follow the general I2C layout guidelines as below:

- Impedance: 50 Ω .
- Topology: Daisy chain.
- Try to keep the total trace length as short as possible.
- To avoid crosstalk for long traces, trace spacing must be $\geq 3x$ in open area.
- Pull-up resistors (one for each of the two signal lines) must be placed at the end of topology.

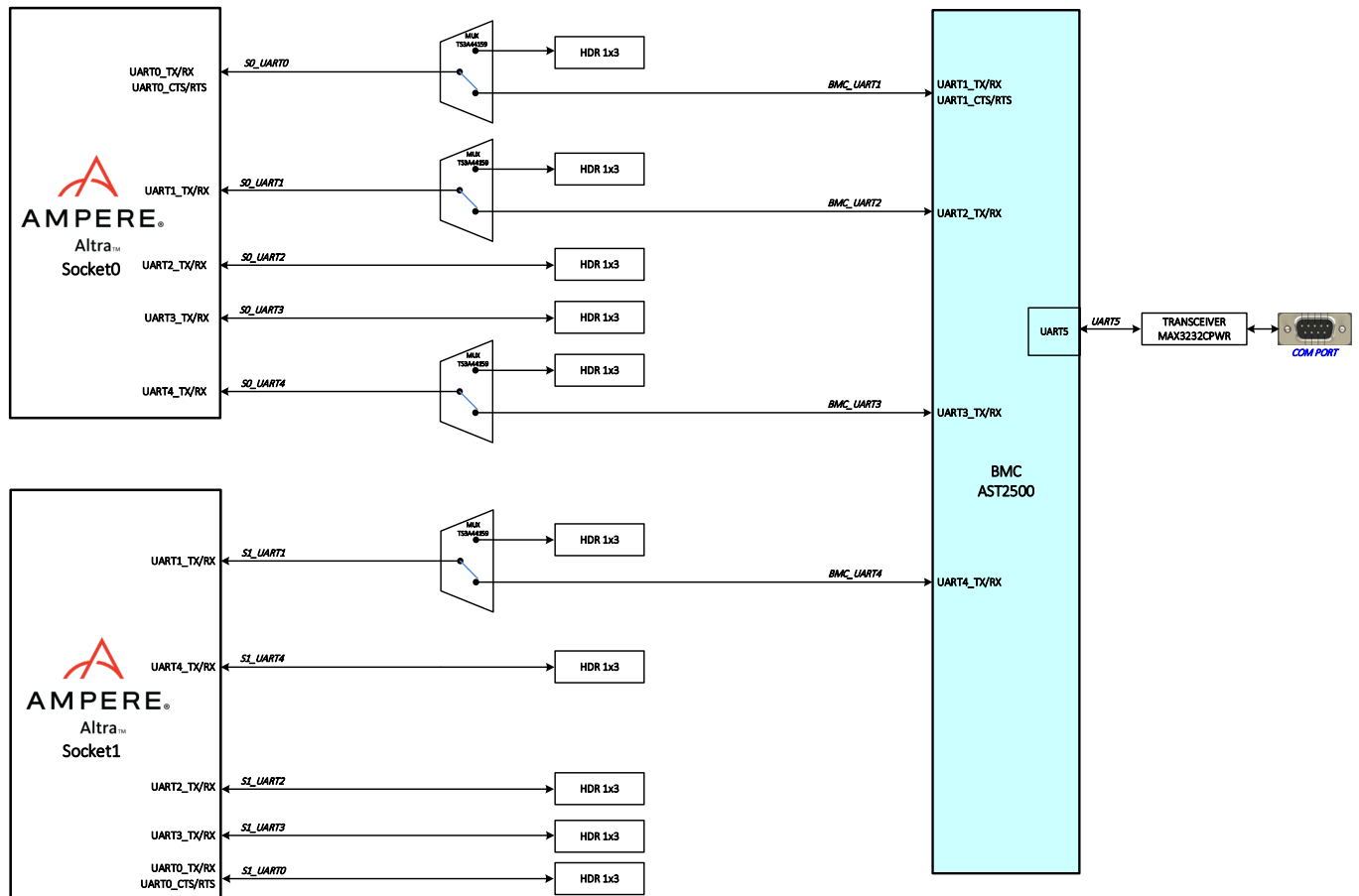


7.2 UART

7.2.1 Design Guidelines

7.2.1.1 Connectivity

Figure 54: UART Block Diagram for Dual-Socket Platforms



Refer to the section titled *Signal Functional Descriptions* in the Altra Datasheet for detailed description of the UART signals.

7.2.1.2 Schematic Guidelines

Altra contains five UARTs, whose assigned functions are listed below:

- Socket0's UART4 is main secure console assigned. Socket1 ATF console is only required if CCIX software is running on both sockets.
- Socket0's UART0 is UEFI and OS console; this must be routed to BMC as well as to header. There is no need for Slave socket.
- UART1 is SMpro console is required for debugging SMpro/PMpro. The goal is to route them to BMC as well as to header. The header option is for the situation where SOL is not working or is not desired.
- UART2: 'Debug console for OS' is used by the Windows debugging tool WinDbg. It is routed to header and connected to WinDbg via UART module.
- UART3: Not used.

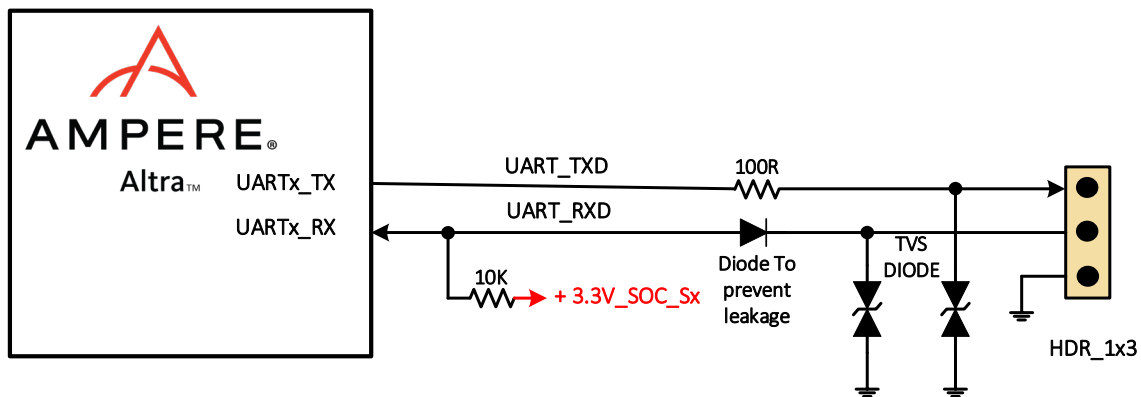


Table 19: Altra UART Allocation

UART	SOCKET0 USAGE	SOCKET0 HEADER	SOCKET0 SoL	SOCKET1 USAGE	SOCKET1 HEADER	SOCKET1 SoL
UART4 (secure)	ATF console	Header	BMC SoL	ATF console	Header	No
UART0	UEFI and OS console	Header	BMC SoL	Not used	Header	No
UART1	SMpro console	Header	BMC SoL	SMpro	Header	BMC SoL
UART2	Debug console for OS	Header	No	Not used	Header	No
UART3	Not used	Not used	No	Not used	Not used	No

- For UART port connected to header, to avoid leakage from outside (such as computer) and for ESD protection, it is recommended to add a 100 Ω serial resistor on the TX line, a diode on the RX line and TVS on both ones.

Figure 55: CPU's 2-Wire UART Connection to Header



7.2.1.3 Termination if Unused

If unused, it is recommended to pull-up UART_RX, UART_CTS, and UART_RTS to +3V3_CPU through a 10K resistor and leave UART_TX floating.



7.3.1.2 Signal Groups

Refer to the section titled *Signal Functional Descriptions* in the Altra Datasheet for detailed description of the SPI signals.

7.3.1.3 Schematic Guides

Altra supports two SPI interfaces – SPI0 and SPI1 with speeds up to 33 MHz.

- The SPI0 bus is used as a boot bus. SPI NOR is connected to SPI0 on CS0 by default.
- If the TPM module shares SPI0 bus with SPI NOR then TPM uses CS1. In this case, SPI1 is free and can be used for Non-Secure devices like Sensors.
- On platforms on which customers need to use TPM on SPI1, both SPI0 and SPI1 are Secure and cannot be used for non-secure devices on either SPI buses.

7.3.2 Termination if Unused

When SPI bus is not used, the SPI_RX must be pulled down to GND through a 220 Ω resistor.

7.3.3 Recommended Devices

The boot SPI NOR flash recommended to be used is Micron MX66L51235FMI, which has a memory size of 512 Mb and 108 MHz (max) clock frequency in single transfer rate (STR) mode. It supports 3-byte and 4-byte addressability modes.



7.4 GPIOs and GPIs

Contains three sets of 8 GPIOs with interrupt capability. Each set (GPIO0-7, GPIO8-15 or GPIO16-23) can be configured as secure or non-secure.

The GPIOs can be configured:

- As inputs in which the pin value is read through registers, or
- As outputs in which the output value and output enable of the pad are controlled through registers.

Note: To mimic an open drain output, the software can set the output value to '0' and drive the output to enable when required to drive a '0' or tri-state the pad when required to drive a '1' (a pull up on the board is needed in this case).

- When configured as an input, the GPIO can be configured to support external interrupt with configurable polarity. Interrupts are routed to GIC, SMpro, and PMpro. The interrupt must be enabled at one of the three destinations.

The GPIs contains 8 general purpose inputs with no interrupt capability in the non-secure world. The signal states must be readable by software via a read-only register. These 8 GPIs cannot route external interrupts to GIC/SMpro/PMpro and cannot be configured as outputs (refer to [Table 20](#)).

Table 20: Altra GPIOs Assignment

Altra GPIO#	S0	S1	SECURITY DOMAIN	DIR FROM Altra	POLARITY	SIGNAL	DESCRIPTION
GPIO_0	–	–	Normal (UEFI/OS access)	–	–	–	ODM/Customer defined use-case
GPIO_1	–	–	Normal (UEFI/OS access)	–	–	–	ODM/Customer defined use-case
GPIO_2	Yes	–	Normal (UEFI/OS access)	INPUT	LOW	RTC_INT_L	– Mt. Jade Reference: Interrupt from RTC device – ODM/Customer defined use-case
GPIO_3	–	–	Normal (UEFI/OS access)	–	–	–	ODM/Customer defined use-case
GPIO_4	Yes	Yes	Normal (UEFI/OS access)	INPUT	HIGH	CPU_BIOS_RECOVER	– Mt. Jade Reference: CPU BIOS recovery – ODM/Customer defined use-case
GPIO_5	–	–	Normal (UEFI/OS access)	–	–	–	ODM/Customer defined use-case
GPIO_6	–	–	Normal (UEFI/OS access)	–	–	–	ODM/Customer defined use-case



Altra GPIO#	S0	S1	SECURITY DOMAIN	DIR FROM Altra	POLARITY	SIGNAL	DESCRIPTION
GPIO_7	Yes	–	Normal (UEFI/OS access)	OUT	LOW	SPI_AUTH_FAIL_L	– Mt. Jade Reference: S0 SPI Authorization Fail report to BMC – ODM/Customer defined use-case
GPIO_8	Yes	Yes	Secure only	OUT	HIGH	FW_BOOT_OK	This is an output from Altra to indicate that SCP boot is successful.
GPIO_9	Yes	N/A	Secure only	OUT	LOW	SHD_ACK_L	The output from host to BMC. Asserted LOW to acknowledge shutdown request from BMC. Altra also asserts this when it completes a soft shutdown request from the OS.
GPIO_10	Yes	N/A	Secure only	OUT	LOW	REBOOT_ACK_L	The output from host to BMC. Asserted LOW to notify BMC that software reboot executed from OS.
GPIO_11	Yes	Yes	Secure only	OUT	HIGH	DDR_SAVE	HIGH output from Altra to trigger NVDIMM #SAVE mode.
GPIO_12	Yes	Yes	Secure only	IN	HIGH	PLIMIT	BMC drives the signal HIGH to Altra to indicate request for power limit.
GPIO_13	Yes	Yes	Secure only	IN	LOW	DDR_ADR	This is an input signal (from BMC) to Altra to handle NVDIMM functionality when a power loss is detected.
GPIO_14	Yes	NA	Secure only	IN	LOW	TPM_ALERT_L	This is an input alert from TPM module.
GPIO_15	Yes	Yes	Secure only	OUT	LOW	SCP_AUTH_FAILURE_L	The output from host to BMC. Asserted LOW to notify BMC of a Secureboot authentication failure.
GPIO_[16:21]	Yes	Yes	Normal (UEFI/OS access)	OUT	LOW	PCIe_Reset_L	Output from host to reset PCIe devices. Altra encodes and CPLD decodes. The PCIe device is reset by sequence.
GPIO_22	Yes	Yes	Normal (UEFI/OS access)	IN	LOW	PCIe_Present_L	Input to host from PCIe Slot. LOW is card present.



Altra GPIO#	S0	S1	SECURITY DOMAIN	DIR FROM Altra	POLARITY	SIGNAL	DESCRIPTION
GPIO_23	Yes	N/A	Normal (UEFI/OS access)	IN	LOW	SHD_REQ_L	The input to host from BMC to request a “graceful shutdown”, LOW level triggered.
GPI_0	Yes	NA	Normal (UEFI/OS access)	IN	HIGH	BMC_OK (BMC Ready)	BMC triggers HIGH level to notify host that it is ready to receive SSIF messages.
GPI_1	Yes	NA	Normal (UEFI/OS access)	IN	LOW	TPM_PRSENT_L	Input to host from TPM Header. LOW means card present.
GPI_2	Yes	Yes	Normal (UEFI/OS access)	IN	HIGH	SPECIAL_BOOT	Active HIGH input to Altra to indicate special boot mode. Special boot mode is used for advanced functionality such as key revocation and programming. Prior to any of the advanced functionality, this pin must be asserted.
GPI_3	Yes	Yes	Normal (UEFI/OS access)	IN	–	JTAG_DAISYCHAIN_DIS	This signal disables internal daisy-chaining of the JTAG DAPs (SMPPro, PMPro, and ARMv8/SoC). 0: All 3 DAPs are daisy chained on the main JTAG port (typically marked “ARMv8” on reference boards). 1: The DAPs are routed to the 3 individual JTAG ports. The main JTAG port routes to the ARMv8 DAP
GPI_4	Yes	NA	Normal (UEFI/OS access)	IN	HIGH	RTC_LOCK	This signal indicates to Altra that RTC access is temporarily restricted. BMC drives this signal HIGH to indicate that it needs access to the RTC.
GPI_[5:7]	–	–	Normal (UEFI/OS access)	IN	–	–	ODM/Customer defined use-case
ALERT_2	Yes	Yes	Secure only	IN	LOW	ALERT2_L	SMBus alert from DIMM (I2C2)
ALERT_3	Yes	Yes	Secure only	OUT	LOW	ALERT3_L	SMBus alert from Altra to BMC



Altra GPIO#	S0	S1	SECURITY DOMAIN	DIR FROM Altra	POLARITY	SIGNAL	DESCRIPTION
ALERT_4	–	–	Secure only	–	LOW	–	Repurposed as a secure GPIO
ALERT_5	–	–	Secure only	–	LOW	–	Repurposed as a secure GPIO
ALERT_6	–	–	Secure only	–	LOW	–	Repurposed as a secure GPIO
ALERT_7	–	–	Secure only	–	LOW	–	Repurposed as a secure GPIO
ALERT_8	Yes	Yes	Secure only	IN	LOW	ALERT8_L	Hot-plug alert event
ALERT_9	Yes	Yes	Secure only	IN	LOW	ALERT9_L	– At boot: S0 asserted to release slave socket – Once slave socket is released, smbalert for I2C9 1) For 2P systems: Must connect directly between the master and slave Altra socket. Note: There should not be a mux in this path. 2) For 1P systems: This controller will be disabled/inaccessible.
ALERT_10	Yes	Yes	Secure only	IN	LOW	ALERT10_L	SMBus alert from DIMM (I2C10)
OVERTEMP	Yes	Yes	Secure only	OUT	LOW	OVERTEMP_L	Output LOW from host to BMC to indicate an OVERTEMP event. The OVERTEMP event causes a power off sequence for the entire SoC to be initiated.
HIGHTEMP	Yes	Yes	Secure only	IN/OUT	LOW	HIGHTEMP_L	Bidirectional: Output when SoC exceeds operational temperature. Input when BMC indicates operational temperature exceeded.
GPIO_FAULT	Yes	Yes	Secure only	OUT	HIGH	GPIO_FAULT	HIGH level-triggered from host to notify BMC that CPU has a fault/non-recoverable error.



Altra GPIO#	S0	S1	SECURITY DOMAIN	DIR FROM Altra	POLARITY	SIGNAL	DESCRIPTION
SYSRESET	Yes	Yes	Secure only	IN	LOW	SYS_RESET_L	The input to host from the BMC or Reset Push button. Asserted LOW to reset host.
SLAVE_PRESENT	N/A	Yes	Secure only	IN/O UT	LOW	SLAVE_PRESENT_L	In a 1P system, this signal is not connected to BMC. In a 2P system, this signal is connected to a BMC and an Altra Master Socket GPIO inputs. It indicates that a Host Slave Socket is present.



7.5 JTAG (Daisy Chain for 2P Systems)

7.5.1 Design Guidelines

7.5.1.1 Connectivity

Altra provides four JTAG ports as debug ports to different Altra JTAG chains: SlimPro, PMPro, SOC, and DAP. All JTAG interfaces are 1.8V. All JTAG ports are directly compatible with Arm JTAG debuggers such as BDI and OCD.

GPI_3 is a dedicated pin “DAISYCHAIN_DIS” to enable or disable three JTAG ports daisy-chained inside Altra: DAP > IPP > PM.

SoC JTAG TAP is separate for engineering debug only.

Figure 57 shows the daisy-chain inside Altra: DAISYCHAIN_DIS = 0 > daisy-chained within Altra as DAP > IPP > PM; DAISYCHAIN_DIS = 1 > Disable daisy-chain. All three port are individually routed outside.

Figure 57: JTAG Daisy Chain Within Altra

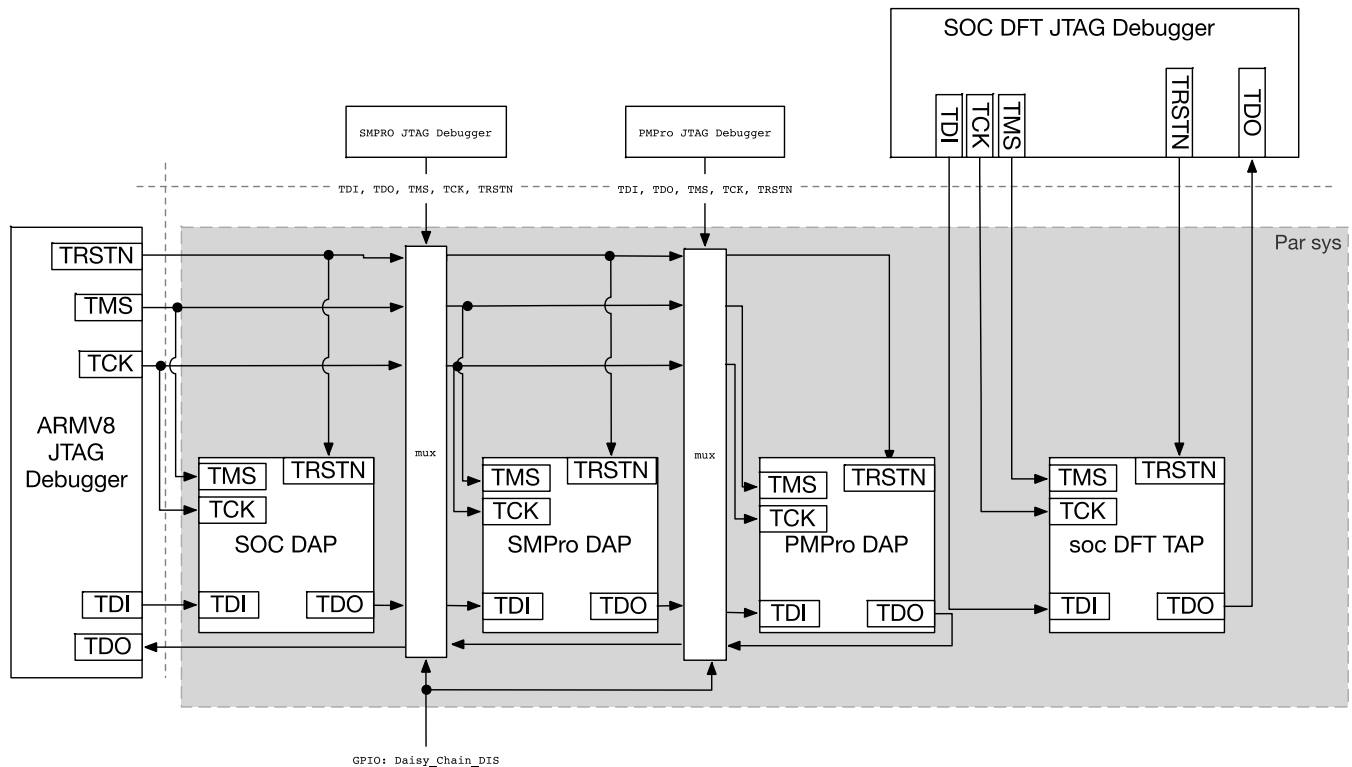


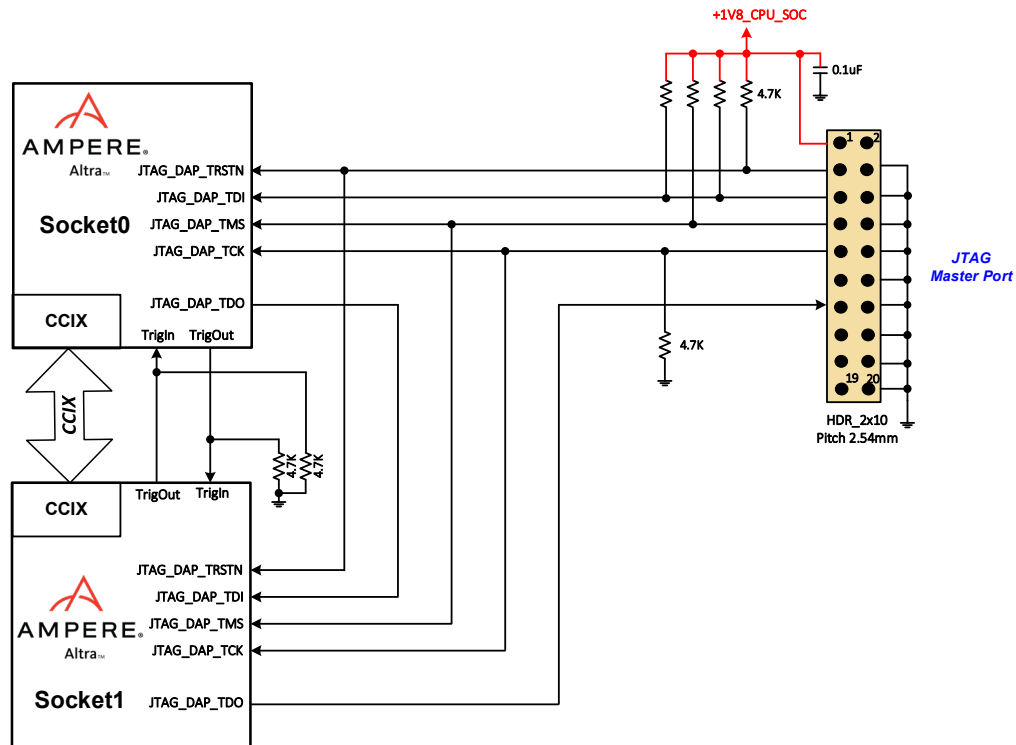


Figure 58 shows the JTAG daisy-chain in a 2P system. In this diagram, internal daisy-chain is enabled. Debug software needs to be aware of this topology and discover the debug capabilities of each socket separately.

Debug triggers between sockets are supported by a set of four trigger inputs (TrigIn[3:0]) and four trigger outputs (TrigOut[3:0]) from each socket.

In single socket systems, TrigIn must be strapped low and TrigOut must be left unconnected.

Figure 58: JTAG Daisy-Chain Connection in 2P Systems



7.5.1.2 Signal Groups

Refer to the section titled *Signal Functional Descriptions* in the Altra Datasheet for detailed description of the JTAG signals.

7.5.1.3 Termination in Normal Operation

Besides JTAG signals, for normal operation, other configuration signals must be connected as below:

Pull-down the following pins using 1K resistors:

- ISOLATE_DIS[1:0]
- JTAG_CMPL[2:0]
- SCAN_EN
- SCAN_MODE
- CAPTURE_EN

Pull-up the following pins to +1.8V_CPU_SOC using 4.7K resistors:

- JTAG_SELECT[3:0]

7.5.1.4 Termination if Unused

If unused, pull-up JTAG_x_TMS/TDI/TDO/TRSTN to +1.8V_CPU_SOC through 4.7 K resistors, pull-down JTAG_x_TCK through 4.7 K resistors.

For details, refer to the section titled *JTAG Interface* in this document.



8. System Boot

On system power-up, BMC boots up first. BMC loads firmware from its main SPI to boot process. If the main SPI firmware is not available or in case of a failover, after 22 seconds, BMC loads the backup firmware stored in the second SPI to boot.

SMpro is responsible for overall system management. One of SMpro's primary responsibilities is to initially boot the system. Altra always boots from an untampered Read-Only-Memory (ROM), and always requires the presence of an external EEPROM attached on SMpro's I2C1 bus at address 0x50 where it loads its 256b bootstrap vector. In Secure boot mode, the bootstrap is loaded from eFuse.

The BMC and CPLD are considered as "always on"; BMC is responsible for turning on/off system power. BMC can also perform a system reboot by asserting SYS_RESET_L. CPLD handles the power-up sequence for both sockets and releases SYS_RESET_L to each Socket when all SOC's power rails are stable.

- Dual EEPROMs (one Main boot and one Failover back-up) are implemented for the firmware image of both sockets. Each socket itself auto-detects whether it is Master or Slave. Master socket loads SMpro firmware and boots first; when boot completes, it notifies Slave Socket by a HIGH output signal on ALERT9_N indicating that SMpro firmware is ready for Slave booting.
- Dual SPI-NOR (one Main boot and one Failover back-up) are also implemented for the UEFI image for the cores for both sockets. Only Altra on Socket0 (Master) can be connected to SPI-NOR for UEFI booting. The Altra on Socket1 (Slave) accesses the SPI-NOR flash via the 2P link.
- Each socket has its own SOC VRM and is enabled by the CPLD. The SOC power plane is considered as Always on for Altra.
- Each socket has its own PCP VRM controlled by its PMpro.
- Each socket manages its DDR DIMMs.
- The BMC controls Altra's SYS_RESET_L.
- SMpro initializes the mesh as well as the 2P link on dual-socket platforms.
- DDR is initialized by Armv8 cores.

Once all voltage rails of the SOC domain and the system reference clock are stable, the CPLD releases the SYS_RESET_L of both sockets.

For detailed Altra boot flow, contact Ampere Computing Support.

8.1 EEPROM Programming and SMpro Boot-up

Refer to [Figure 59](#). The following two subsections describe the UEFI programming and boot-up sequences.

8.1.1 EEPROM Programming Sequence

1. BMC turns off the chassis.
2. BMC outputs BMC_SPI0_PROGRAM_SEL= 0; => The BMC takes over the I2C1 bus for programming
3. BMC outputs BMC_I2C_BACKUP_SEL = 0 or 1 depending on user selection to switch I2C bus to main or failover boot EEPROM and then upgrade one or both EEPROMs.
4. After EEPROM upgrading is complete, BMC restores BMC_SPI0_PROGRAM_SEL and BMC_I2C_BACKUP_SEL to leave I2C1 bus to Socket0. BMC powers up the board.



8.1.2 SMpro Boot-up Sequence

1. On power up, once all voltage rails of the SoC domain and the system reference clock are stable, the BMC/CPLD releases S0_SYS_RESET_L. Note that Socket1 is still under reset.
2. By default, Master Socket (Socket0) accesses the EEPROM and boots-up first.
3. Socket0: When SMpro boot is completed, ALERT9_N is driven HIGH and ALERT3_N is driven LOW.
4. For the ALERT9_N signal:
 - a. If ALERT9_N is wired to BMC/CPLD: A HIGH output on ALERT9_N indicates to BMC/CPLD to release S1_SYS_RESET_L.
 - b. If ALERT9_N is not wired to BMC/CPLD: If GPIO8=0 (SCP_FW_BOOT_OK), the falling edge of ALERT3_N indicates to CPLD to release S1_SYS_RESET_L.

Note: ALERT3_N is a dual-purpose pin, depending on the boot phase:

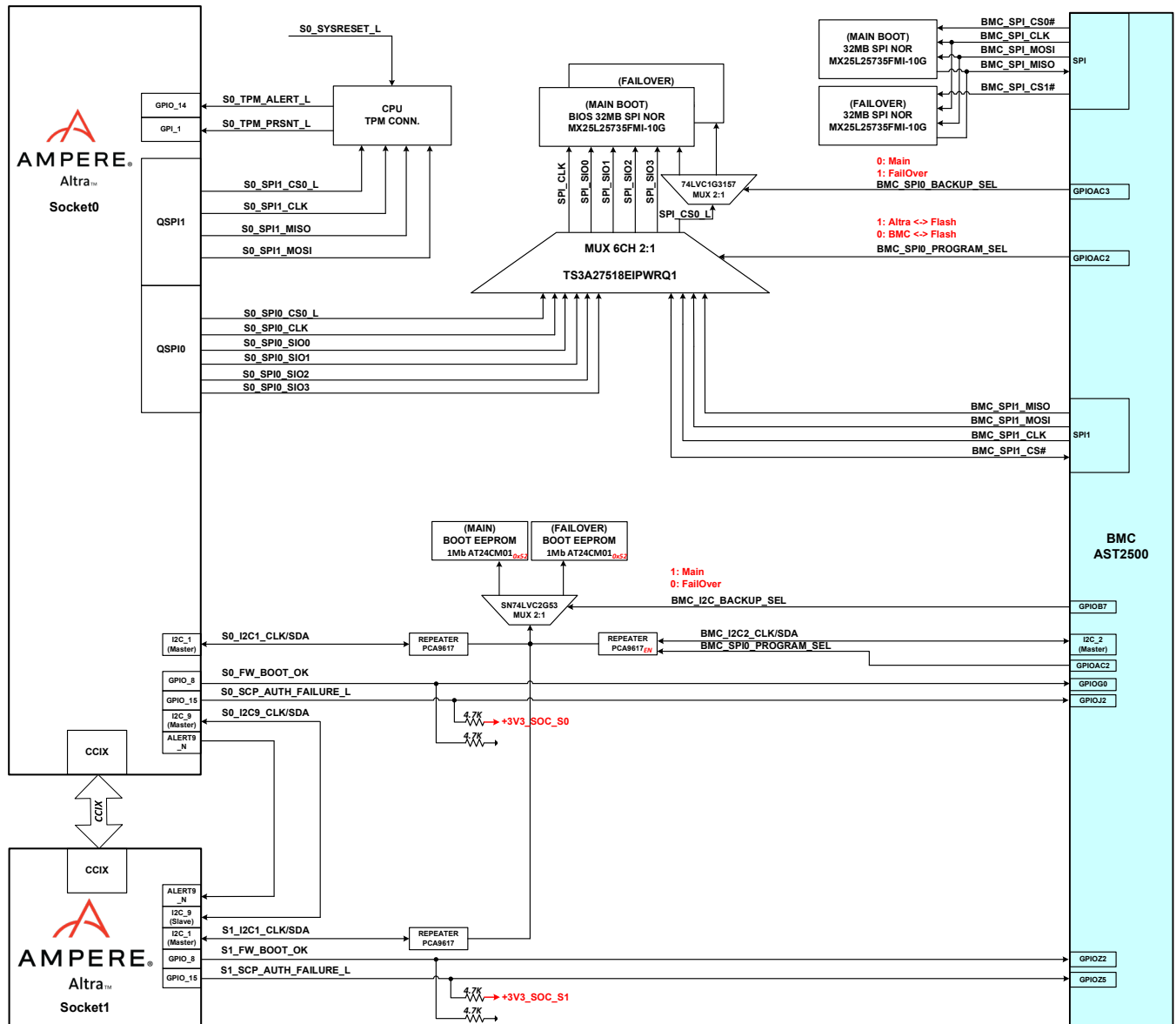
1. If GPIO8=0 (SCP_FW_BOOT_OK), ALERT3_N is used as described above.
2. If GPIO8=1 (SCP_FW_BOOT_OK), ALERT3_N is connected to BMC/CPLD as an SMB ALERT signal from Altra.
5. Socket0 outputs a HIGH on S0_FW_BOOT_OK to indicate to BMC/CPLD that Socket0 boot has completed.
6. When Socket1 boot is completed, Socket1 outputs a HIGH on S1_FW_BOOT_OK to indicate to BMC/CPLD that Socket1 boot has completed.

If, after a predefined amount of time (which the software must specify), when BMC/CPLD software checks level status of Sx_SCP_AUTH_FAILURE_L:

- 0: Means SMpro boot failure, BMC/CPLD needs to control BMC_I2C_BACKUP_SEL to switch to failover EEPROM and reset Altra.
- 1: Means SMpro booted successfully.



Figure 59: System Boot for Dual-Socket Platforms





8.2 UEFI Programming and Boot-up

Refer to [Figure 59](#). The following two subsections describe the UEFI programming and boot-up sequences.

8.2.1 UEFI Programming Sequence

1. BMC turns off the chassis.
2. BMC outputs BMC_SPI0_PROGRAM_SEL= 0; => BMC owns SPI bus for upgrading
3. BMC outputs BMC_SPI0_BACKUP_SEL = 0 or 1 depending on user selection to select the main or failover SPI NOR flash and then upgrade one or both EEPROMs.
4. After UEFI upgrading is done, BMC restores BMC_SPI0_PROGRAM_SEL and BMC_SPI0_BACKUP_SEL to switch SPI bus to Socket0. BMC turns on the board.

8.2.2 UEFI Boot-up Sequence

1. On power up, after SMpro boots up completely, UEFI boots up
2. Socket0 owns the SPI bus for UEFI booting
3. Socket1: UEFI booting is through CCIX.
4. Socket0 and Socket1 boot up in parallel and wait for a sync point.
5. During boot-up, Socket0 and Socket1 exchange messages via I2C9.
6. When Socket1 boot is complete, Socket1 sends a message to Socket0 via I2C9 that boot has completed.



9. Hardware Bring-up Guide

9.1 Component Inspection Checks

Note: Non-populated (NOPOP) components must be verified as per the assembly Bill of Materials (BOM).

9.2 Power Supply and GND Short Checks

Use a digital multimeter/multitester (DMM) to measure the resistance between the listed power rail and GND (see [Table 21](#)). If any power rail shows the resistance as 0 Ω , it indicates a voltage short to GND for that rail. Refer to the documentation for your board to determine the test point for each rail.

Table 21: VCC and GND Short Checks (Unit: Ω)

POWER RAIL	TEST POINT	IMPEDANCE (Ω)	POWER RAIL	TEST POINT	IMPEDANCE (Ω)
+5V_SB			+2V5_BMC		
+1V8_CPLD			+1V05_USB_HUB		
+12V			+3V3_SB/+3V3_CPLD		
+3V3_VRD_S0			+3V3		
+5V_VRD_S0			+5V		
+0V75_VDDC_SOC_S0			+3V3_VRD_S1		
+0V85_VDDC_RCA_S0			+5V_VRD_S1		
+1V8_SOC_S0			+0V75_VDDC_SOC_S1		
+2V5_VPP0123_S0			+0V85_VDDC_RCA_S1		
+2V5_VPP4567_S0			+1V8_SOC_S1		
+1V8_VDDH_S0			+2V5_VPP0123_S1		
+1V5_VDDH_S0			+2V5_VPP4567_S1		
+3V3_SOC_S0			+1V8_VDDH_S1		
+1V2_VDDQ0123_S0			+1V5_VDDH_S1		
+1V2_VDDQ4567_S0			+3V3_SOC_S1		
+0V6_VTT0123_S0			+1V2_VDDQ0123_S1		
+0V6_VTT4567_S0			+1V2_VDDQ4567_S1		
+0V75_PCP_S0			+0V6_VTT0123_S1		
+1V8_PCP_S0			+0V6_VTT4567_S1		
+1V2_BMC			+0V75_PCP_S1		
+1V15_BMC_CORE			+1V8_PCP_S1		



9.3 Power Rails Checks

Measure the voltages on all power supply rails and fill in the measured results in the **Measured Value** column in [Table 22](#). Ensure that all values are within the **Min – Max** range.

Note: **G** indicates Good; **NG** indicates Not Good.

Table 22: Mainboard Power Rails' Voltage Measurement

POWER RAIL	TOLERANCE	TEST POINT	MIN (V)	MAX (V)	MEASURED VALUE	G/NG
+5V_SB	5%		4.75	5.25		
+3V3_SB	5%		3.135	3.465		
+1V8_CPLD	5%		1.71	1.89		
+12V	5%		11.4	12.6		
+5V	5%		4.75	5.25		
+3V3	5%		3.135	3.465		
+3V3_VRD_S0	5%		3.135	3.465		
+5V_VRD_S0	5%		4.75	5.25		
+0V75_VDDC_SOC_S0	5%		0.675	0.825		
+0V75_PCP_S0	0.75 – 1.1 V		0.75	1.1		
+1V2_VDDQ0123_S0	5%		1.14	1.26		
+1V2_VDDQ4567_S0	5%		1.14	1.26		
+0V6_VTT0123_S0	5%		0.57	0.63		
+0V6_VTT4567_S0	5%		0.57	0.63		
+2V5_VPP0123_S0	5%		2.375	2.625		
+2V5_VPP4567_S0	5%		2.375	2.625		
+0V85_VDDC_RCA_S0	5%		0.8075	0.8925		
+1V8_VDDH_S0	5%		1.71	1.89		
+1V5_VDDH_S0	5%		1.425	1.575		
+1V8_SOC_S0	5%		1.71	1.89		
+3V3_SOC_S0	5%		3.135	3.465		
+1V8_PCP_S0	5%		1.71	1.89		
+3V3_VRD_S1	5%		3.135	3.465		
+5V_VRD_S1	5%		4.75	5.25		
+0V75_VDDC_SOC_S1	5%		0.675	0.825		
+0V75_PCP_S1	0.75 – 1.1 V		0.75	1.1		
+1V2_VDDQ0123_S1	5%		1.14	1.26		
+1V2_VDDQ4567_S1	5%		1.14	1.26		



POWER RAIL	TOLERANCE	TEST POINT	MIN (V)	MAX (V)	MEASURED VALUE	G/NG
+0V6_VTT0123_S1	5%		0.57	0.63		
+0V6_VTT4567_S1	5%		0.57	0.63		
+2V5_VPP0123_S1	5%		2.375	2.625		
+2V5_VPP4567_S1	5%		2.375	2.625		
+0V85_VDDC_RCA_S1	5%		0.8075	0.8925		
+1V8_VDDH_S1	5%		1.71	1.89		
+1V5_VDDH_S1	5%		1.425	1.575		
+1V8_SOC_S1	5%		1.71	1.89		
+3V3_SOC_S1	5%		3.135	3.465		
+1V8_PCP_S1	5%		1.71	1.89		
+1V2_BMC	5%		1.14	1.26		
+1V15_BMC_CORE	5%		1.093	1.208		
+2V5_BMC	5%		2.375	2.625		
+1V05_USB_HUB	5%		0.996	1.103		
PQT_VDM_EXTVREF	0.5%		0.6965	0.7035		

9.4 Power Sequence Measurement

Measure the power sequence for all power rails and verify this sequence against the designed sequence shown in [Figure 37](#).

9.5 Clock Signals Checks

Measure the frequencies of all clock signals on the mainboard and fill in the measured results in the **Measured Value** column in [Table 23](#). Refer to the documentation for your board to determine the test point for each clock signal.

Note: G indicates Good; NG indicates Not Good.

Table 23: Mainboard Clock Frequency Measurement

CLOCK SIGNAL NAME	DESIGN VALUE	TEST POINT	MEASURED VALUE	G/NG
CLK1M8432_SO_UART_REF_R	1.8432 MHz			
CLK1M8432_S1_UART_REF_R	1.8432 MHz			
RTC_XTAL_IN/OUT	32.768 KHz			
CLK25M_9FGL0841_XI/XO_R	25 MHz			
CLK25M_TMR_R	25 MHz			
CLK25M_CPLD	25 MHz			
CLK100M_SO_SYS_REF_SRNS_P/N	100 MHz			
CLK100M_S1_SYS_REF_SRNS_P/N	100 MHz			
CLK100M_SO_RCB1B_OA_REF_P/N	100 MHz			



CLOCK SIGNAL NAME	DESIGN VALUE	TEST POINT	MEASURED VALUE	G/NG
CLK100M_S0_RCB1A_0B_REF_P/N	100 MHz			
CLK100M_S1_RCA2_REF_P/N	100 MHz			
CLK100M_S1_RCB1A_0B_REF_P/N	100 MHz			
CLK100M_S1_RCB2B_3A_REF_P/N	100 MHz			
CLK100M_S1_RCB2A_3B_REF_P/N	100 MHz			
CLK100_S1_X24_REF_P/N	100 MHz			
9ZXL1231_REF_P/N	100 MHz			
CLK100M_BMC_PCIE_REF_P/N	100 MHz			
CLK100M_uPD_PCIE_REF_P/N	100 MHz			
CLK100M_NVME1_PCIE_REF_P/N	100 MHz			
CLK100M_NVME2_PCIE_REF_P/N	100 MHz			
CLK100M_S0_RCA3_1_REF_P/N	100 MHz			
CLK100M_S0_RCB3A_0_REF_P/N	100 MHz			
CLK100M_S0_RCB2B_0_REF_P/N	100 MHz			
CLK100M_S0_RCA2_1_REF_P/N	100 MHz			
CLK100M_S0_RCA2_2_REF_P/N	100 MHz			
CLK100M_S1_RCB0A_REF_P/N	100 MHz			
CLK25M_CPLD_R	25 MHz			
CLK100M_S0_SYS_REF_SRIS_P/N	100 MHz			
CLK100M_S1_SYS_REF_SRIS_P/N	100 MHz			
CLK25M_TMR	25 MHz			
CLK25M_5P35023_XO_R	25 MHz			
CLK24M_uPD_X1/X2	24 MHz			
CLK25M_ETH_PHY_XO/XI	25 MHz			
CLK50M_OCP_NCSI	50 MHz			
CLK50M_BMC_NCSI	50 MHz			
CLK24M_BMC	24 MHz			



10. Bibliography

- Altra Architecture Specifications
- Altra Debug Architecture Specifications
- Altra I/O List
- Altra Clocking Overview
- Altra Power Sequencing
- Altra Reset Specifications
- Altra TSM Design Specifications
- Altra BMC Interface Specifications
- Altra Software Overview



11. Document Revision History

ISSUE	DATE	DESCRIPTION
1.00	January 20, 2021	Updated the following: - Sections 4.1.1.2, 4.1.1.3, 4.1.1.4, 4.1.1.5, 4.4 - Minor fixes and corrections.
0.95	December 23, 2020	Minor updates and fixes.
0.90	October 30, 2020	Updated the following: Figure 3, Figure 22, Figure 24, Figure 32, Figure 33, Figure 34, Figure 35, Figure 36, Figure 37, Figure 38, Figure 40, Figure 41, Figure 44, Figure 52, Figure 56, Figure 58, Figure 59 Table 7, Table 20, Table 22 - Section 4.1.1.2, 4.1.1.3, 4.1.1.5, 4.2.1, 4.3.1, 4.4.1, 8.1.2 - Updated the value of Z_{target} (up to 1 MHz) to 2 mΩ in section 4.1.1.3 - Updated the value of Z_{target} (0 to 1 MHz) to 2 mΩ in section 4.4.1.2 Minor fixes and corrections
0.80	April 10, 2020	Updated the following: - Product name from eMAG 2 to Altra - Sections 2.4, 2.5, 4.4, 5.2.1, 7.4 Added the following: Chapter 9 - Minor fixes and corrections.
0.70	July 24, 2019	Updated the following: - Sections 4, 8 Figure 12, Figure 13, Figure 14, Figure 18, Figure 22, Figure 25, Figure 34, Figure 35, Figure 50, Figure 52, Figure 53, Figure 59 Table 20 Added the following: - Section 5.2
0.60	June 19, 2019	Updated the following: - Sections 1.2, 4.2, 4.3 Figure 14, Figure 22, Figure 33, Figure 35, Figure 50, Figure 51, Figure 56, Figure 59 Table 3 Added the following: Figure 18
0.53	May 07, 2019	Updated the following: - Sections 1.1, 2.3.1, 3.1.2.3, 4, 5.1.3, 0, and 7.5.1.3 Figure 3, Figure 5, Figure 12, Figure 17, and Figure 37
0.52	April 10, 2019	Updated the following: - Sections 1.9, 3.1.2.10, 3.1.2.11, 3.2, 5.2, 7.4, 7.5, 8 Figure 13 and Figure 17



ISSUE	DATE	DESCRIPTION
0.42	February 20, 2019	- Deleted the section titled “19-Inch 1U/2U Server Platforms” - Deleted the section titled “Thermal and Mechanical Design” - Corrected the signal names within SPI section - Added note for simulation images - Added Altra’s GPIO table (Table 20) in section 7.4
0.41	February 19, 2019	- Changed the document titled from “Platform Hardware Specification” to “Platform Hardware Design Specification” - Added hardware design guides for each section
0.40	January 30, 2019	- Incorporated comments and feedback post team review. - Added Chapters 2, 3, 4, 5, 5.2, and 8. - Updated the contents for Chapter 7.
0.31	December 12, 2018	Incorporated comments and feedback post team review.
0.30	November 15, 2018	Updated the document template.
0.20	October 24, 2018	Updated the following: - Altra reference clock scheme - AST2500 BMC block diagram for single-socket and dual-socket platforms - System boot - I/O interfaces between two sockets and BMC - Power Supply Design (updated detailed power rails) - BMC subfunctions
0.10	September 28, 2018	Initial release.



January 20, 2021

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